Smart Ultraviolet Sensor for Hydrogen Flame Detector Application based on Neuro-OEIC and FPGA

ニューロOEICとFPGA技術を基にした水素火炎検知用スマート紫外光センサ

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Abstract

Title	Smart Ultraviolet Sensor for Hydrogen Flame Detector Application based on Neuro-OEIC and FPGA ニューロOEICとFPGA技術を基にした水素火炎検知用スマート紫外光センサ

It is important to have a continuous monitoring system for detecting a hydrogen flame in industries, laboratories, or residential area to prevent further damages. Detecting a hydrogen flame in daylight at a wide observation area is difficult since the hydrogen flame produces a pale blue color and generates less heat, but emits UV-C radiation. By exploiting the application of the optoelectronic integrated circuits (OEIC), a smart UV sensor for detecting a hydrogen flame is proposed. This doctoral thesis presents a study on a smart UV sensor for hydrogen flame detector application by three-dimensional (3-D) integration between a neuro-OEIC and an FPGA to realize a chip with small form factor and low-power consumption.

The smart UV sensor not only detects the hydrogen flame but also delivers the information about the location, speed, direction, and spreading status of the hydrogen flame. The smart UV sensor contains of three parts: focal plane array (FPA) of UV-sensitive photodiodes, complementary metal oxide semiconductor (CMOS) circuit as a readout circuit and an edge detection circuit (EDC), and the motion object detection circuit implemented in the field-programmable gate array (FPGA). The neuro-OEIC that mimics the outer vertebrate retina combines the FPA and EDC to extract the edge of the detected object for acting as a preprocessing unit. While the FPGA is used as an image analyzer.

Previous research in our laboratory fabricated a backside-illuminated Schottky barrier diode Pt/n^--$Al_{0.49}Ga_{0.51}N$ on sapphire as the UV focal plane array. The photodiode has a size of 250 μm x 250 μm with a pitch of 500 μm. The leakage current was 10^{-13} A at -3.0 V bias with an ideal factor of 1.14. Under illumination, the photodiode showed a photocurrent of 8 x 10^{-11} A with the responsivity of 2 x 10^{-4} A/W at a radiation power of 6.4 μW/mm^2. This reveals that the external quantum efficiency of the fabricated photodiode was ~0.1%. In near

future, the external quantum efficiency of the photodiode will be expected increasing up to 10%. Thus, the photodiode will produce photocurrent in a range of 14.1 fA - 14.1 nA.

The motion object detection circuit in the FPGA utilized histogram projection to determine the object's position within the image. The image is projected vertically and horizontally. Both edges of the projected object are located to get the size of the object. From those edges, other information is derived such as the centroid, speed, direction, and spreading status of the object. A two-dimensional array of 250 x 250 pixels was simulated to evaluate the system's calculation of the speed and direction of the given object. The execution time of the implemented circuit in the Spartan-6 XC6SLX25 FPGA device was 0.05 ms. Thus, the implemented circuit in the FPGA might process the images up to 20,000 frames/s.

The hydrogen flame was targeted to occur as a spurt with a height of 5 m with a flame speed of 100 m/s at 10 m away from the sensor. An optical subsystem such as a convex lens with a focal length of 3 mm might be added to have a better focused object as well as increasing the photon flux received by the focal plane array. Using the fabricated focal plane array, the minimum number of the pixel required to detect the targeted hydrogen flame is 3 x 3 pixels. In this stage, the CMOS circuit was fabricated and wired-integrated with the motion object detection circuit implemented in the FPGA to evaluate the calculation of the object's flame speed. The photocurrents were simulated using a microcontroller that was programmed to generate moving patterns. The one-dimensional array CMOS circuit of 1 x 16 pixels was fabricated with 1.5 μm process technology using 5 micron lambda rules. The silicon diode as the readout circuit has a size of 50 μm x 50 μm with a forward voltage of 0.58 V and a leakage current of 0.64 nA at -1.0 V bias. The MOS transistor has a width and a length of 15 μm and 10 μm, respectively. The NMOS has a threshold voltage of 1.6 V with a saturation current of 0.3 mA at a V_{GS} of 5.0 V and a V_{DS} of 3.0 V. The PMOS has a threshold voltage of -1.6 V with a saturation current of -0.13 mA at a V_{GS} of -5.0 V and a V_{DS} of -3.0 V. The fabricated EDC chip can detect the given photocurrent in a range of 100 nA - 50 μA with V_{DD} of 5 V, V_{OFS} of 2.2 V, and V_{TH} of 2.2 V. The wired-integrated system was evaluated to calculate the object with a speed in range of 0.86 – 1,957.8 pixels/s which is equal to an actual flame speed of 1.43 - 3,263 m/s.

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Chapter 1

Introduction

1.1 Motivation

Nowadays, hydrogen not only is widely used in the industries, but also is used in our fuel cell based vehicles, buildings, offices, laboratories, as well as our home. At the fiscal year of 2015, Japan's government has been starting the Hydrogen Society. This means that the hydrogen is a primary source to generate electricity and to power vehicles. This is to address the issue of reducing the fossil fuel dependencies as well as the green house gasses emission. The illustration of the Hydrogen Society concept is shown in Figure 1.1. [1–4] In the hydrogen production cycle (from manufacture, storage, distribute, and usage to the users), a leakage could become a problem. When hydrogen gas is released and mixed with the air, hydrogen gas may self-ignite. [5] Before the hydrogen gas is ignited, there are hydrogen gas detectors for early warning if the leakage of

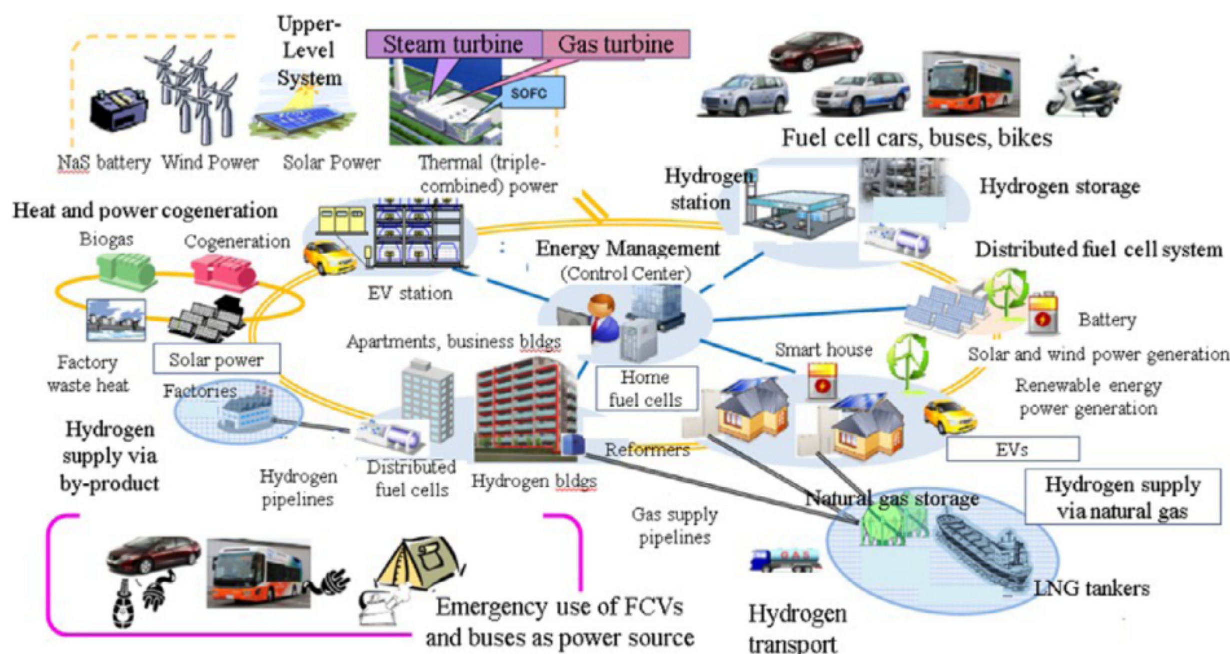


Figure 1.1: Hydrogen Society concept in Japan. *Source*: Chihiro Tobe, ANRE, METI, 18 September 2013. Translated by Noriko Behling, Mark C. Williams, and Shunsuke Managi. [4]

Figure 1.2: Hydrogen flame visibility in daylight (left) and at night (right) comparing with propane flame. *Source: https://h2tools.org/bestpractices/h2introduction/hazards/flames*

hydrogen gas occurs. A resistance-based hydrogen gas sensors are widely used. [6] The resistance of the material changes when it is exposed to the hydrogen gas. Other hydrogen gas sensor is a chemochromic tape which is used by NASA. [7] The tape changes its color when is exposed to a hydrogen gas. The material is based on palladium oxide (PdO) and titanium oxide (TiO_2) class of pigments. However, when the hydrogen gas is ignited, another detector should be used. It is a hydrogen flame detector. The hydrogen flame is not visible in daylight condition, emits less heat, but it radiates a strong ultraviolet (UV)-C radiation. [8,9] Figure 1.2 shows the visibility comparison between hydrogen flame and propane flame in daylight and at night. A UV-C wavelength has a solar-blind properties which lays on a wavelength of 200 – 280 nm. [10,11] Thus, detecting a UV-C radiation at sea-level even outside in daylight can be realized.

Some examples of available hydrogen flame detector in the market are shown in Figure 1.3, along with its wavelength response information. The UVTRON R2868 and the photomultiplier tube R10601 only detect the presence of a hydrogen flame. In a wider observation area, they can not tell where the location of the hydrogen flame is. The S4111-46Q photodiode array and the UV camera ICX407BLA have array configuration that can be used for pointing the location of the hydrogen flame. However, they still need a processing unit such as computer systems to acquire the captured images and then displaying or analyzing the images.

This research aims at the development of smart UV sensor that integrates a processing unit on-chip to have a small dimension as well as low power consumption. The proposed smart UV

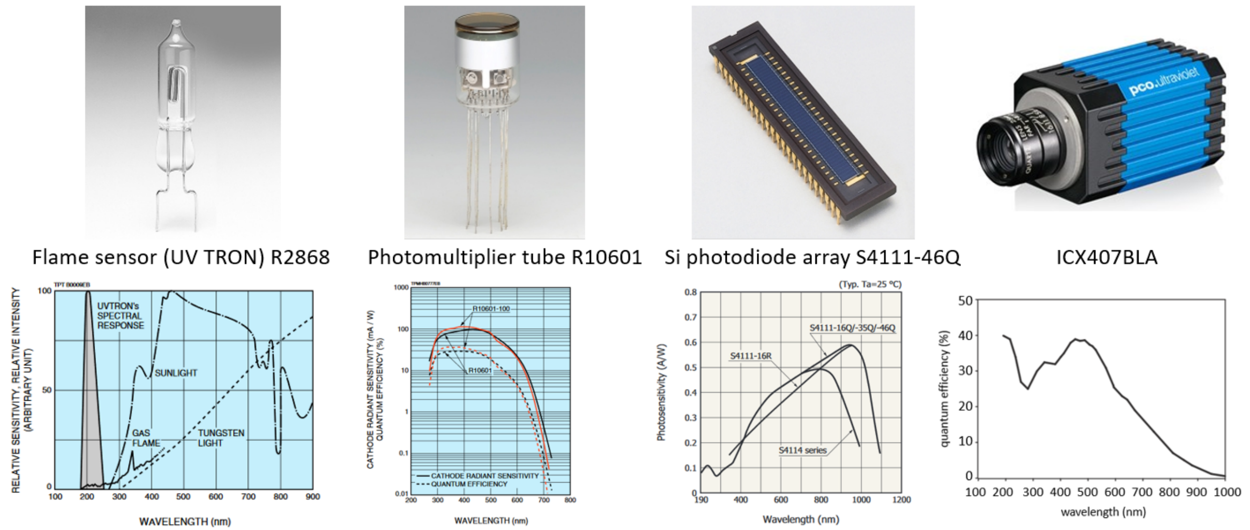


Figure 1.3: Example of available UV sensors. (a) Flame detector by Hamamatsu Photonic K.K. (b) UV photomultiplier by Hamamatsu Photonic K.K. (c) One-dimensional array of 46 x 1 pixels by Hamamatsu Photonic K.K. (d) UV CCD camera system from PCO-TECH Inc.

sensor not only detects the hydrogen flame, but also generates information such as the location, size, speed, direction, and spreading status of the hydrogen flame. The speed is related to the flame speed of the hydrogen flame. The direction is where the hydrogen flame mostly moved. The spreading status is whether the flame expands, steady, shrinks, or disappears. The smart UV sensor extends the application field of the fabricated UV focal plane array that was developed in our laboratory. The information generated by the smart UV sensor is also designed to be sufficiently fit as the Internet of Things (IoT) device.

1.2 Problem definition

Before designing the smart UV sensor, the problem definitions in this research are stated as follows:

1. Giving a spurt of hydrogen flame with a height of 5 m and a speed of 100 m/s at 10 m away from the sensor.
2. The sensor captures the UV-C radiation from the hydrogen flame, performs a necessary preprocessing, and produces binary images.
3. The binary images are analyzed by the FPGA as the main processing unit to generate useful

information such as the presence, location, size, speed, direction, and spreading status of the hydrogen flame in real-time.

This thesis also considered that in flame analysis field, it is necessary to identify the flame edges. [12, 13] The flame edges provide a basic quantitative decision of shape, stability, size, and location of the flame. The flame edges reduce the amount of data processing as well, while maintain the shape (boundaries) of the flame. In addition, hydrogen flame is categorized as a high-speed object. Having a shorter processing time is important. Thus, there are some addition problems for designing the smart UV sensor as follows:

1. Extracting the flame edges for further analysis.
2. Transferring the image data from the sensor to the processing unit as fast as possible.

1.3 Related works

This section gives a glimpse of previously presented studied on smart sensor, ultraviolet photodetector, neuro-OEIC, FPGA processing circuit, and the 3-D integrated circuit technology.

1.3.1 Smart sensor

Smart sensor is defined as sensor that is capable of generating digital output, executing logical function, performing two-way communication, and making decision. [14–16] To be smart, a sensor does not have to be integrated. [16] A smart sensor has four units, namely a sensor device, an analog front end, an analog-to-digital (A/D) converter, and a digital processor, as shown in Figure 1.4. [17] Examples of smart sensor are MMA8451Q 3-axis accelerometer from NXP Semiconductors and

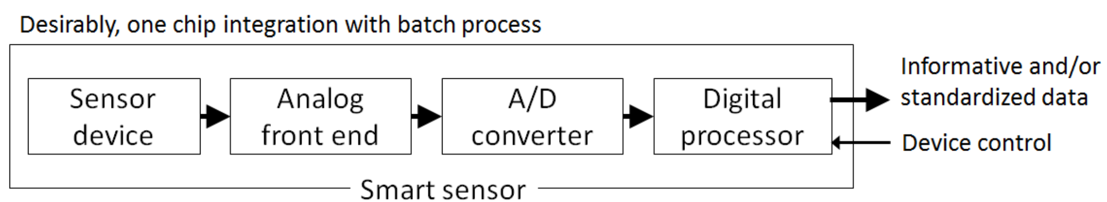


Figure 1.4: Smart sensor concept [17]

ADNS3080 high-performance optical mouse sensor from Avago Technologies. The MMA8451Q contains a processor that is capable of detecting free-fall, detecting shake through motion threshold, and detecting single, double, or directional tap. [18] The ADNS3080 is able to determine the direction and relative distance of motion, in which is mostly used as mice for desktop personal computer (PC). [19] In this thesis, we would like to integrate the processor unit that is capable to generate useful information related to the detected hydrogen flame such as the location, size, speed, direction, and spreading status.

1.3.2 UV-C photodetector

A hydrogen flame contains ultraviolet (UV), visible and infrared radiation. Indeed, a hydrogen flame is not completely colorless. But, the color of a hydrogen flame is pale blue and sometimes yellow color also occurs, so it difficult to see especially in the daylight. [20] A hydrogen flame also emits heat, but less heat is produced comparing to a hydrocarbon flame. To take advantage of a hydrogen flame detector, one should consider about the background signal which mostly comes from the sun.

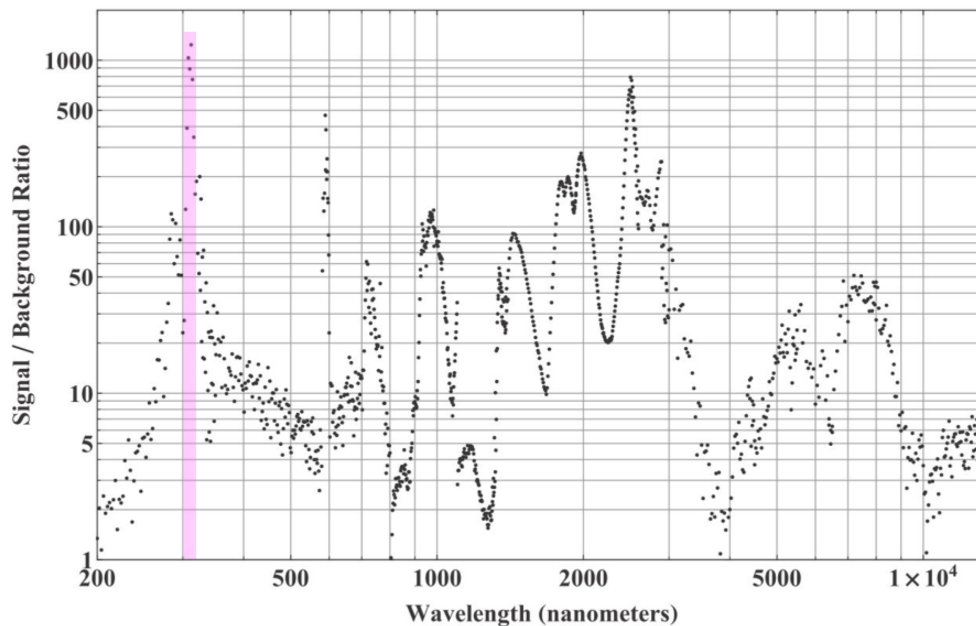


Figure 1.5: The ratio of the hydrogen flame to the background signal. [21] The peak ratio is at 309 nm (shown in the pink-bar)

The ratio of a hydrogen flame to the background signal, which is taken with and without the

hydrogen flame, was reported as Figure 1.5. [21] In Figure 1.5, the hydrogen flame has a peak at 309 nm, which lays at the ultraviolet radiation bands (UV < 400 nm). Three major subtypes of ultraviolet wavelengths are UV-A (320-400 nm), UV-B (280-320 nm), and UV-C (200-280 nm). From a total solar radiation that reach earth's surface, only around 7%-9% is ultraviolet radiation. [22] From that portion, it contains of 95% UV-A and 5% UV-B. [23] Meanwhile, UV-C is completely absorbed by oxygen molecules in the ozone layer in our atmosphere. This means, at the earth's surface, there is no UV-C coming from the sun as background signal. In this case, a UV-C detector is also called as solar blind detector. It makes us easier to make a hydrogen flame detector for sensing the UV-C radiation generated by a hydrogen flame, even outside in the daylight condition, with assumption there is no artificial UV-C radiation that might be interfered, for example from mercury lamps or arcs inside the detection area.

Silicon based solar-blind ultraviolet photodetectors have been widely used because they are easy to be fabricated. Silicon has a bandgap of 1.13 eV, meaning that the cut-off wavelength of silicon is 1.1 μm which lays in the far infrared spectrum. By using a silicon as ultraviolet photodetector, one should add a filter to block the radiation beyond ultraviolet wavelength. A filter of Fabry-Perot-type Al-SiO_2-Al is an example as the interference filter used for silicon based ultraviolet photodetector. [24] However, using an additional filter means additional cost and complexity in fabrication. This reason leads to the usage of the wide bandgap materials. [25] A wide bandgap material has a cut-off wavelength at the ultraviolet wavelength, meaning that it is sensitives only to the ultraviolet radiation intrinsically without an additional filter. Appendix A describes the basic calculation of the silicon wavelength range.

In III nitride group there are GaN and AlN, as well as its ternary compound such as InGaN and AlGaN. The In molecules in InGaN device adjust the cutoff wavelength from 1.8 μm to 365 nm. InGaN based devices has been reported had a high leakage current and strong PPC (persistence photoconductivity) owing to a high density dislocations. [26] Meanwhile, the Al molecules in AlGaN device tune the cutoff wavelength from 210 nm to 360 nm. Previously growing an AlGaN was difficult, but recently AlGaN is grown onto AlN as the template on sapphire substrate to avoid crack and absorption loss. [26] It is also reported that for a bigger Al mole, the responsivity decreases due to lower material quality. [27] Fabricating GaN ultraviolet photodiodes on the silicon substrate has been done to enable optoelectronic devices. [28] Back-side illuminated AlGaN based focal plane arrays have been demonstrated and flip-chip bonded with the readout circuit. [29–33] Figure 1.6 shows the relation between the Al concentration, the bandgap energy, and the cut-off wavelength in the AlGaN compound. It shows that to fabricate a solar blind photodetector, the Al concentration should be higher than 40%.

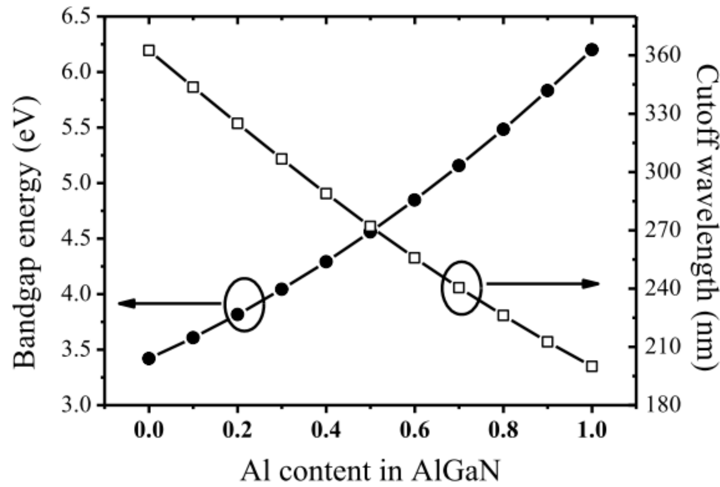


Figure 1.6: Bandgap energy and cut-off wavelength relationship with the Al concentration in the AlGaN [26]

Non III nitride based ultraviolet devices includes Diamond, SiC, and other oxides. Diamond has a bandgap of 5.5 eV but the grain boundaries and non-diamond impurities reduce the photoresponse. It also reported that making an n-type diamond is also complicated because the diamond lattice is very small and rigid. [26] SiC has a bandgap of 2.0 eV until 7.0 eV, therefore additional filter is needed to have a specific wavelength range. [26] ZnO was reported having a slow response speed because the absorption and dis-absorption of oxygen molecule near its surface. [34] A various wide bandgap semiconductor nano-materials such as SnO_2, ZnS, ZnSe, In_2Te_3, TiO_2, MoS_2, Nb_2O_5, $NiCo_2O_4$, Ga_2O_3, $K_2Nb_8O_{21}$, and Zn_2GeO_4 indicate a promising material as a ultraviolet photodetector. Those nano-materials took an advantages of low cost and simple manufacturing and showed higher responsivity and photoconductivity gain because they have high surface are-to-volume ratios. [35] β-Ga_2O_3 on p-type silicon substrate showed enhanced photoelectric responsivity that enables optoelectronic devices. [36]

Currently in our laboratory, we are developing III nitride materials. The focal plane array AlGaN based of 4 x 4 pixels has been fabricated by Akinari Takada and Barry Ousman 1. [37, 38] The sample structure consists of a 300 μm Sapphire substrate, then 100 nm AlN buffer layer, followed by 1500 nm $n^+-Al_{0.64}Ga_{0.36}N$ contact layer, and 400 nm $n^--Al_{0.49}Ga_{0.51}N$ active layer. A 100 nm Platinum was used as the Schottky metal and four layers (Ti/Al/Ti/Au) Ohmic contact at a thickness of 140 nm. For the contact, a 500 nm Au pad was used. The Platinum is also used to reflect the incident light back to the active layer. The AlN buffer layer and the Sapphire substrate are transparent to the incident light. The sensing area of one photodiode was 250 x 250 μm^2 with 500 μm pitch between the center of two adjacent photodiodes. Figure 1.7 shows the fabricated

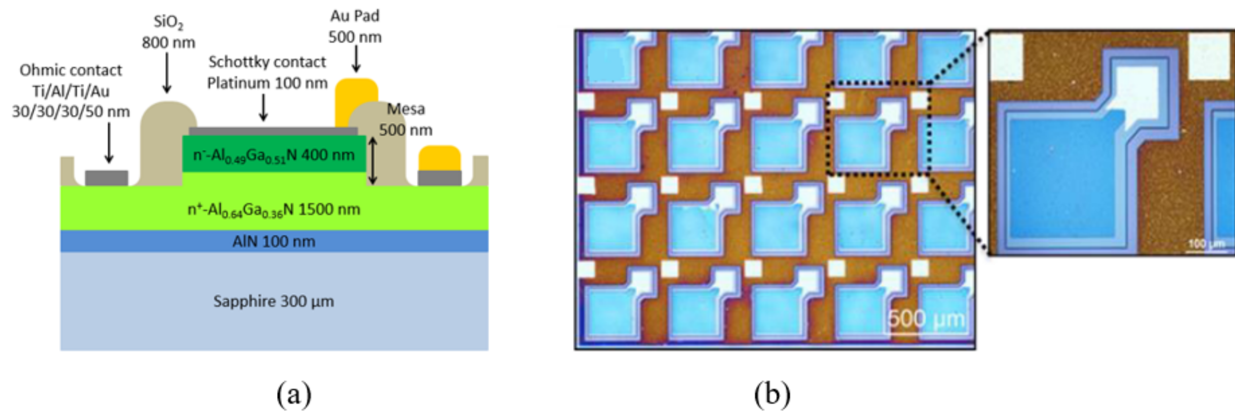


Figure 1.7: The development of photodiode array in our laboratory. (a) The cross section of the pixel. (b) Focal plane array chip [38]

photodiode array in our laboratory and Figure 1.8 shows the I-V characteristic under the illuminated condition. Under the dark condition, the photodiode generated a very low leakage current at 10^{-13} A. A low leakage current meaning that the device can detect a low power of ultraviolet radiation. Moreover, the ideal factor estimation of the photodiode (n) is 1.14 which is near the ideal factor of an ideal diode ($n = 1$). Thus, a diode characteristic was confirmed on the fabricated photodiode. In the illuminated condition with the ultraviolet wavelength of 296 nm and the radiation power of 6.4 μW/mm^2, the photodiode showed a photocurrent of 8×10^{-11} A and a resistivity of 2×10^{-4} A/W. In this stage, the efficiency of the photodiode was $\sim 0.1\%$. The shifting of the cross section between reverse bias and forward bias from 0 V to 1 V was due to the charge traps in the depletion region that might be created during fabrication processes or caused by crystal defects. In addition,

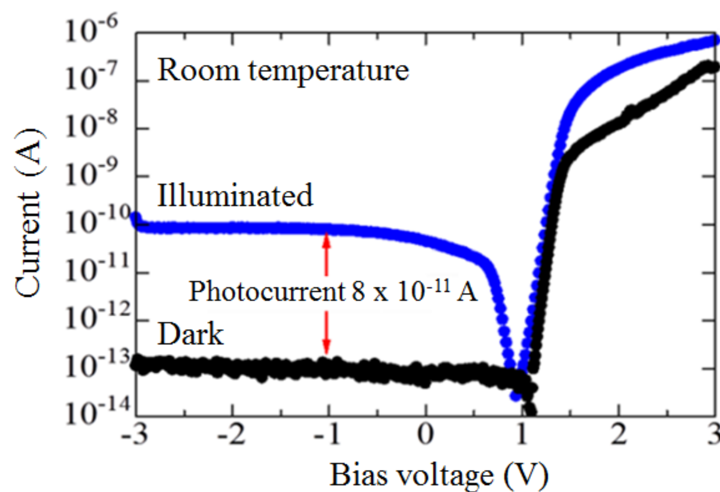


Figure 1.8: The I-V characteristic under illuminated condition [38]

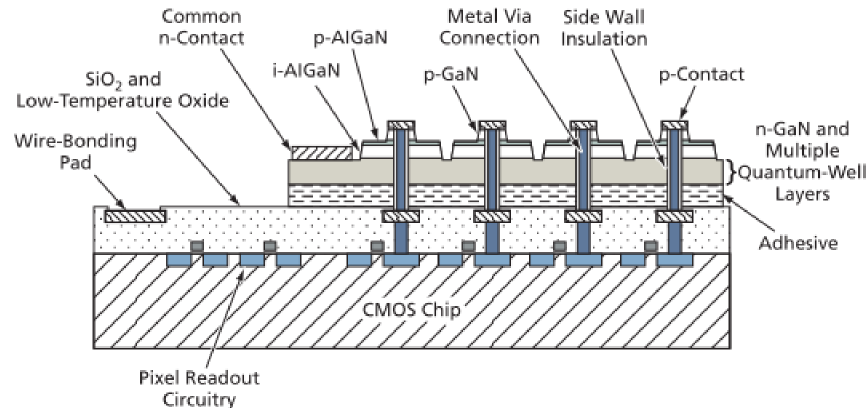


Figure 1.9: Hybrid UV image sensor with via structure [40]

above the bias voltage of 1.25 V in the forward bias, the current line bends, which shows that the current is limited by series resistance within the photodiode structure. The photodiode calculation is described in Appendix B.

The Schottky barrier diode (SBD) UV photodiode was chosen because it has advantages that are easy to fabricate the structure using a standard CMOS process, having a fast response, showing a little persistent photoconductivity, and able to make as a back-side illuminated (BSI) configuration. [39] The BSI SBD UV photodiode is also easy to be stacked with the CMOS circuit without via structure. As a comparison, photodetector with p-i-n structure requires via structure to be stacked with the CMOS circuit, as demonstrated by Xinyu Zheng and Bedabrata Pain of Caltech for NASA's Jet Propulsion Laboratory in Figure 1.9.

1.3.3 Neuro-Optoelectronic integrated circuit

The terminology of neuromorphic system was introduced by Carver Mead to express analog devices that imitate neurobiological structure in the nervous system. [41] Whereas, optoelectronic integrated circuit (OEIC) is technologies that integrate the photonic devices and electronic circuits monolithically or heterogeneously. As a Neuro-OEIC, we would like to integrate a focal plane array with edge detection circuits which mimic the outer vertebrate retina. A heterogeneous integration of focal plane array of ultraviolet photodetectors with readout circuit has been demonstrated using indium-bump flip-chip bonding. [29–33] However, they did not implement the neuromorphic system, therefore pixel-by pixel or column-by-column readout mechanism was used which became our first problem to be addressed. Meanwhile, edge detection circuits based on outer vertebrate retina have been developed but their application did not involve the ultraviolet photodetector. [42–45]

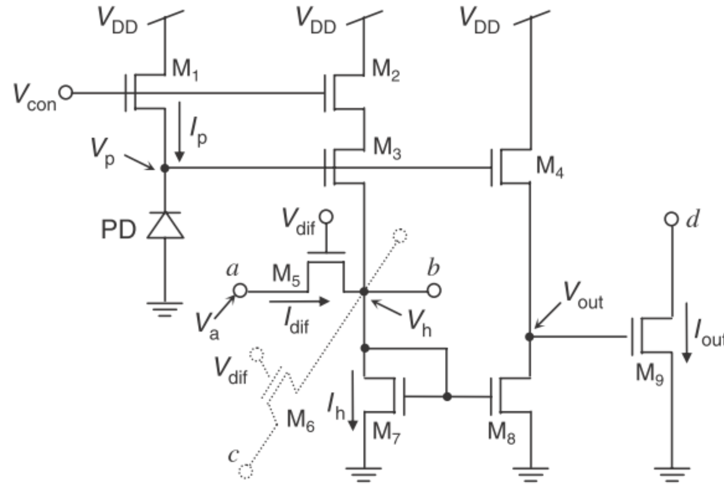


Figure 1.10: A unit circuit of edge detector circuit [45]

In this thesis, we integrated the focal plane array of ultraviolet photodetectors onto the edge detection circuit as a neuro-OEIC. The edge detection circuit was originally developed by K. Nishio with a unit circuit as shown in Figure 1.10. [45] The photocurrents generated by the photodetectors was passing through a silicon diode and an NMOS transistor. Then, the edge detection circuit produces a spike-like current signal at the edge positions. Finally, a fixed threshold current was applied to digitize the output current into binary voltages that is ready to be connected with the FPGA as the main processing circuit.

1.3.4 FPGA motion detector circuit

The optical flow technique has been used for detecting the motion of an object. [46–49] A computer vision method designed by Horn & Schunck was implemented on an FPGA device for images at a resolution of 256 x 256 pixels with a frame rate of 257 fps. [46] Another computer vision algorithm, Lucas & Kanade's method, was applied on an FPGA device for images at a resolution of 320 x 240 pixels with a frame rate of 30 fps (frame per second). [47] Meanwhile, a biological inspired algorithm-based using Elementary Motion Detection (EMD) principle was made on an FPGA device for images at a resolution of 12 x 1 pixels with a maximum frame rate of 5,000 fps as micro-air vehicle application. [48] The elaborated EMD by adding logarithmic transformation to minimize the sensitivity of the incident light was implemented into an FPGA device for images at a resolution of 256 x 256 pixels with a frame rate of 350 fps. [49] However, by using those techniques, after the optical flow calculation was performed, each pixel has a vector

(speed and direction), then one should take the resultant of all vectors of the corresponding object to decide the real vector of the object which would be complicated to implement.

In this thesis, we used an easy technique for taking the resultant by implementing a projection histogram algorithm which projects the image vertically and horizontally, then after finding the edges of each projected image, other information can be obtained, i.e. the centroid of the object within the frame (the image area), size of the object as a rectangular shape, speed of the object, direction of the object, and status of the object whether the object expands, steady, shrinks, or disappears.

1.3.5 3-D integrated circuit

A three-dimensional integrated circuit (3-D IC) is an IC with more than one plane of devices and metals, connected by vertical interconnects (such as through-silicon vias or TSVs). 3-D integration technology has four advantages. The first is to reduce of the interconnect wire length to improve wire latency and to reduce power consumption. The second is to improve memory bandwidth by stacking memory on microprocessor cores with massive vertical connections between the memory layer and the core layer. The third is to realize heterogeneous integration, which can promote new architecture designs. The fourth is to have a smaller form factor, which results in higher packing density and smaller foot-print. [50] 3-D integration is also an alternative solution for the need of higher bandwidth as well as the silicon scaling which is getting more difficult and expensive. [51] Sony was fabricated their 3-D imaging sensor in 2012, which stacked the BSI focal plane array onto the CMOS circuit, to achieve a faster speeds. [52] Toshiba also announced their

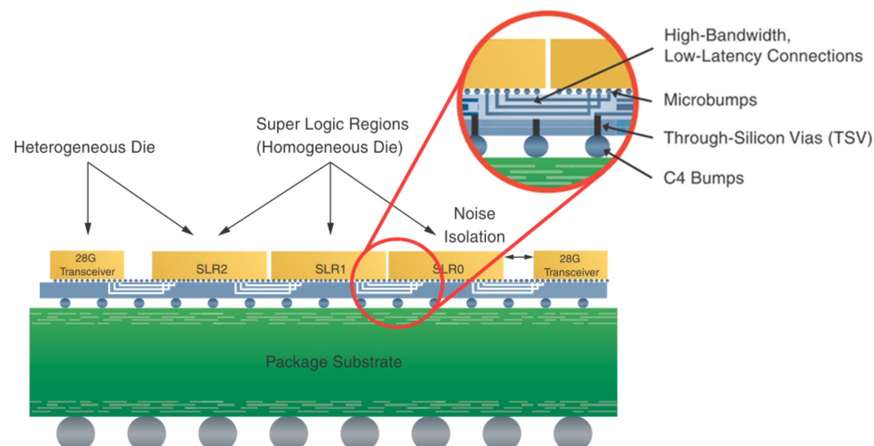


Figure 1.11: Heterogeneous 3-D FPGA from Xilinx Inc. [54]

48-layer 3-D bit cost scalable (BiCS) flash memory in 2015 for realizing a high density storage. [53]

In 2011, Xilinx Inc. introduced the first commercially available 2.5-D integrated system architecture FPGA device XC7V2000T with the Stacked Silicon Interconnect (SSI) technology as shown in Figure 1.11. [54] The SSI technology integrates homogeneous or heterogeneous dies onto the silicon interposer. The silicon interposer is an electrical interface routing between one chip/die or to another. By taking the advantage, this thesis would like to stack the neuro-OEIC circuit and the FPGA.

1.4 Design concept

The smart UV sensor was designed to locate the position of a hydrogen flame within a two-dimensional observation area. By following the concept of smart sensor in Figure 1.4, the smart UV sensor's units are the Pt/n$^-$-Al$_{0.49}$Ga$_{0.51}$N BSI-SBD photodiode array as the sensor device, the silicon diode as the readout circuit, the CMOS-based EDC as the preprocessing unit that generates binary images, and the FPGA as the image analyzer that produces the information related to the detected hydrogen flame, as shown in Figure 1.12.

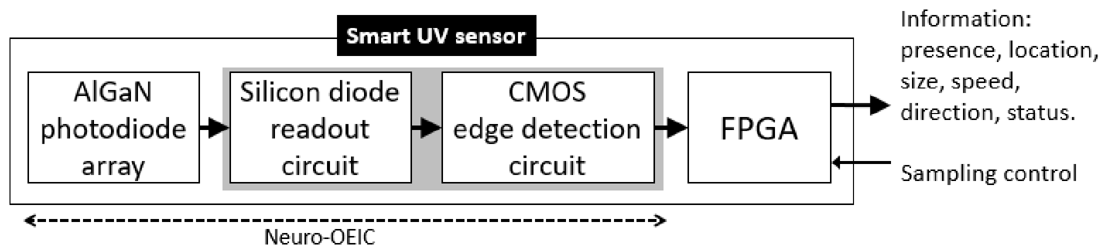
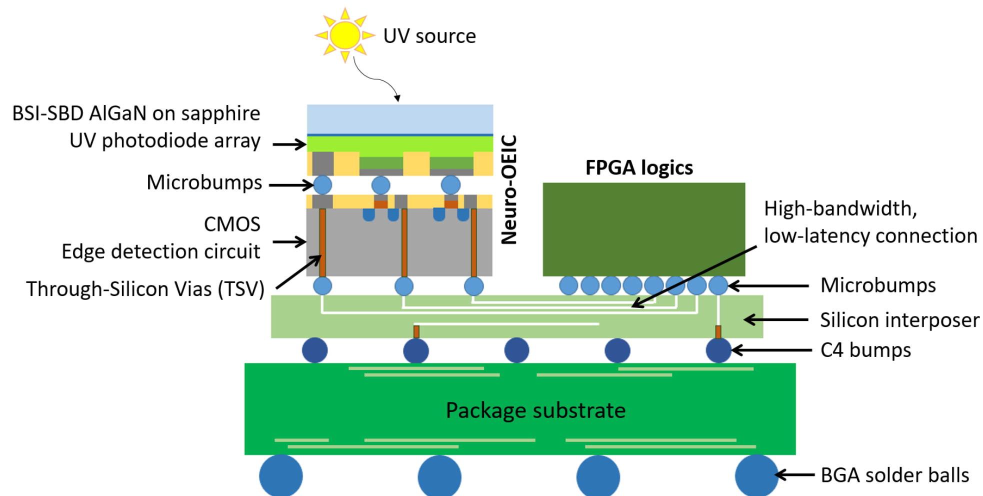


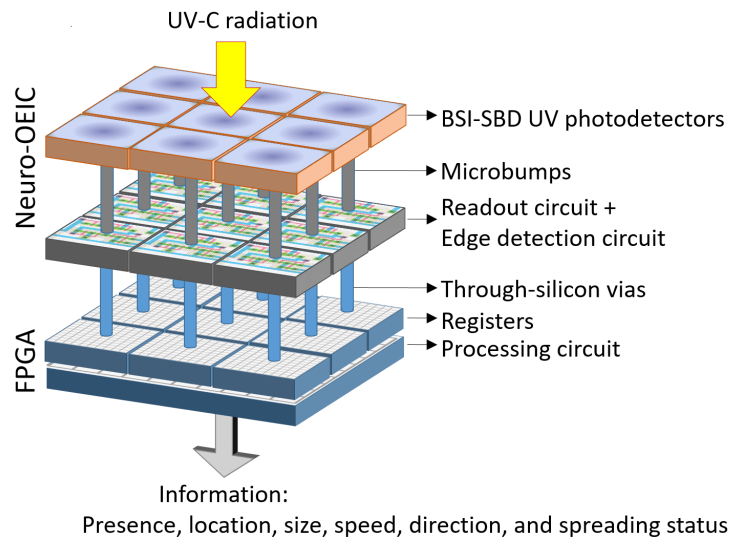
Figure 1.12: Proposed smart UV sensor's units

Addressing the requirements that is described in section 1.2, the proposed smart UV sensor introduces a 3-D integration system architecture between the neuro-OEIC and the FPGA. The neuro OEIC has a function as edge detection preprocessing unit, the FPGA is the main processing unit that analyses the images, while the 3-D architecture makes the parallel data transfer possible. Having a preprocessing unit is very useful for reducing the tasks in main processing unit. Therefore, the edge detection function was not performed in the FPGA. Instead, the edge detection function was implemented as an analog circuit.

This thesis proposes an integration concept between the neuro-OEIC and the FPGA as shown



(a)



(b)

Figure 1.13: Integration concept between the neuro-OEC and the FPGA with (a) 2.5-D/3-D integration with the SSI technology or (b) true 3-D integration

in Figure 1.13. By utilizing the SSI technology, the outputs of the neuro-OEIC are connected to the FPGA logics via a silicon interposer as illustrated by Figure 1.13(a). When the FPGA vendor allows a custom vertical stacking with heterogeneous dies in the future, we would like to have an integration structure as shown in Figure 1.13(b).

1.5 Objectives and design specifications

At this stage, the fabricated BSI-SBD UV photodiode array is not used. Therefore, the main goals of this thesis are as following:

1. Fabricate the silicon diode and edge detection circuit base on the previously fabricated UV photodiode' design. For a concept of demonstration, a one-dimensional array of 16 pixels was fabricated.
2. Implement a simple motion object detection in the FPGA base on histogram projection to generate information such as the presence, location, size, speed, direction, and spreading status.
3. Evaluate the flame speed calculation of the wired-integration system between the fabricated silicon diode with edge detection circuit and motion object detection in the FPGA.

The CMOS circuit, which contains the silicon diode and edge detection circuit, and the motion object detection circuit in the FPGA were designed by considering the design specifications base on the previous fabricated BSI-SBD UV photodiode array and some prerequisites. The design specifications are listed in Table 1.1.

1.6 Contribution

This thesis contributes to the field of optoelectronic integrated circuit and its application for hydrogen flame monitoring purposes. It advanced the knowledge in the following ways:

1. Present a brief but systematic study of the application of the neuro-OEIC and the FPGA as a hydrogen flame detection and analysis.
2. Develop a simple motion object detection based on histogram projection in FPGA to locate an object within the image and to measure the speed of the object.
3. Produce examples for calculating the sensor resolution and converting the real speed to the pixel speed.

4. Provide a report about a 2.5-D/3-D integration between OEIC and FPGA as a smart sensor.
5. Contribute the know-how of a CMOS fabrication using standard process for improving the curriculum in Electronic Engineering Polytechnic Institute of Surabaya.

Table 1.1: Design specifications guidance

Smart UV sensor design specifications	
Flame to sensor distance	10 m
Radiation power	10 pW/mm^2 – 10 μW/mm^2
Hydrogen flame speed	100 m/s
Hydrogen flame height	5 m
Lens focal length	3 mm
Fabricated BSI-SBD UV photodiode array	
Pixel size	250 $\times$ 250 μm^2
Pixel pitch	500 μm
Photocurrent (η=10%, no lens)	14.1 fA – 14.1 nA
Minimal design requirements for the CMOS circuit and FPGA	
Input current range of the edge detection circuit	14.1 fA – 14.1 nA
Number of pixel in a row	3 pixels
Detected object speed	60 pixel/s

1.7 Thesis organization

This thesis is organized as follows.

Chapter 2 gives an introduction about device processing technology especially related to a standard CMOS processes which was used to fabricate the edge detection circuit in this thesis.

Chapter 3 describes the design and simulation of the edge detection circuit which were

fabricated on a silicon wafer along with the silicon diode as the readout circuit. A one-dimensional array of 1 x 16 pixels was fabricated to demonstrate the concept.

Chapter 4 shows the design and simulation of the histogram projection based motion object detection circuit in the FPGA. The binary image of 250 x 250 pixels was generated by the personal computer.

Chapter 5 reports the integration of the fabricated edge detector circuit chip and the motion object detection circuit in the FPGA using wires. The integration system was evaluated for the speed calculation in which the photocurrent was generated by the microcontroller.

Chapter 6 summarizes the research as a whole and describesthe important points concluded from it. It also identifies a few aspects that can be improved as a guidance for probable future works.

Chapter 2

Device fabrication processing technology

2.1 Introduction

Fabricating a metal oxide semiconductor (MOS) devices to form an integrated circuit need a repeating process. Commonly, a pure bulk silicon is used as the base or the substrate where the devices lay on it. This pure bulk silicon is called as wafer. The wafer goes through a multiple photo lithography process and some chemical processing steps. Those processing steps can be categorized as deposition, removal, patterning and modification of electrical properties. The processing technology is advancing due to the requirements of the device scaling and to reduce the process variations. This chapter briefly discusses about the simplified application specific integrated circuit (ASIC) design flow and the equipments utilized in this thesis.

2.2 ASIC design flow, cross section, and process flow

Semiconductor device fabrication is the process to make the integrated circuits that are exist in everyday electrical and electronic devices. Semiconductor device fabrication uses multiple-step sequence of photolithograpy and chemical processing steps to create electronic circuits on a wafer made of pure semiconducting material. Silicon is mostly used, but several compound semiconductors (III-V group, for instance) are used for specialized applications. A simplified ASIC design flow is shown in Figure 2.1.

For designing the schematic and layout of the CMOS circuit, we used an open-source computer-aided design program called Electric from Static Free Software, a division of RuLabinsky Enterprises Inc. [55] The designed circuit was simulated using a free software LTspice from Linear Technology. [56] The simulation program with integrated circuit emphasis (SPICE) parameter level 3 from our laboratory was used to simulate the CMOS circuit.

The CMOS circuit was fabricated with 1.5 micron technology, while the layout was design

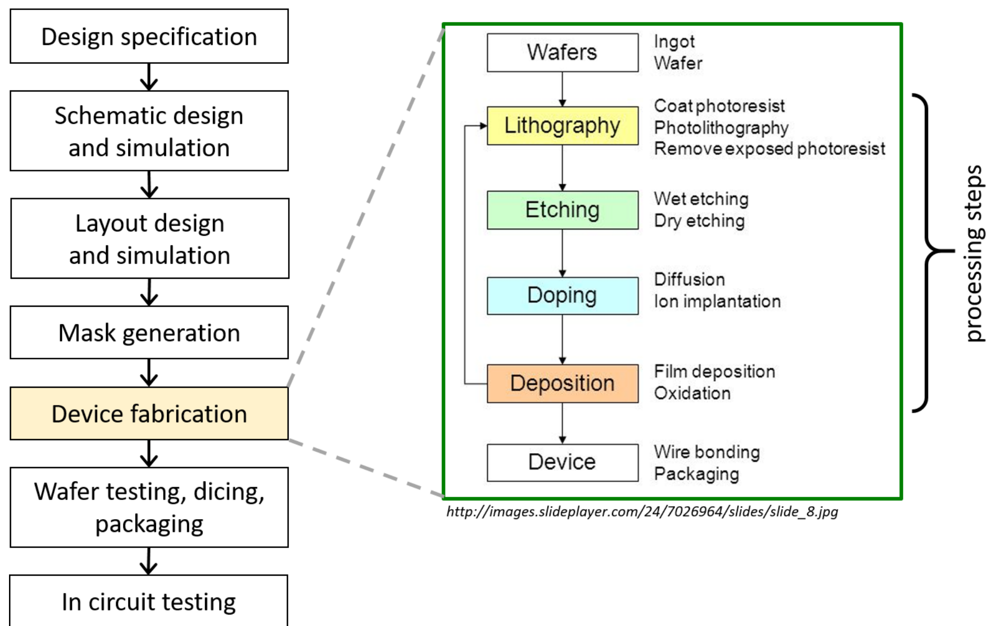


Figure 2.1: Simplified ASIC design flow

using 5 micron design rules. The cross section of the CMOS circuit is shown in Figure 2.2. The legend shows the layer's name and the recipe for the fabrication process. The designed CMOS circuit required 11 masks including the mask for the alignment mark. The substrate was using 2-inch Boron-doped wafer with the crystal orientation of <100> and the resistivity of 1.49 $\sim$ 1.63 Ω.

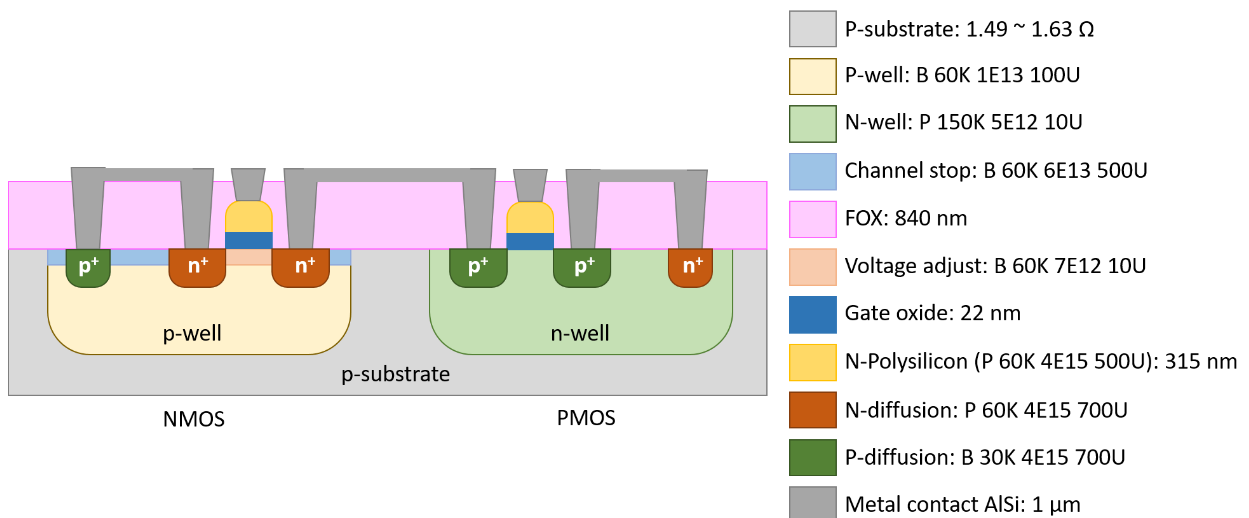


Figure 2.2: Cross sectional of the CMOS circuit

The main group of the process flow is shown in Figure 2.3. To fabricate the designed CMOS circuit, it required a total of 57 processing steps. The mask generation, processing steps of device fabrication, and testing are briefly explained in the following sections.

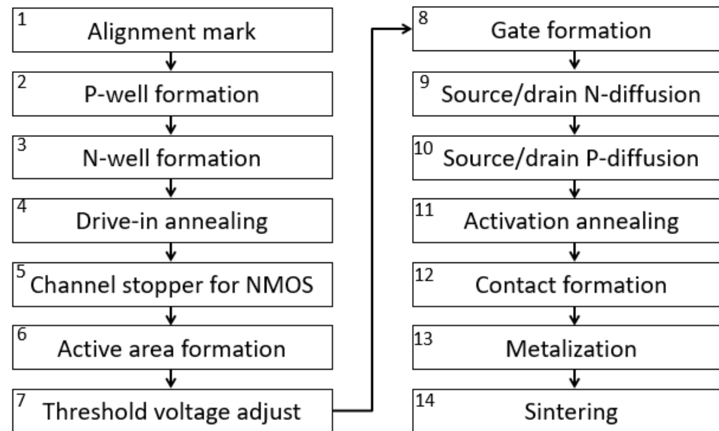


Figure 2.3: Main process flow of the designed CMOS circuit

2.3 Vacuum technology

Many of MOS fabrication processes are carried out in partial vacuum condition. Partial vacuum condition is a condition at pressure order magnitude below ambient atmospheric pressure (up to 13 orders of magnitude). Generally speaking, vacuum is a space with completely free of matter. But there is no such a "absolute-vacuum" condition. in consequences, an atmosphere with a pressure under ambient is called "partial-vacuum", or simply called as "vacuum". Table 2.1 shows the definition of vacuum degree related to the pressure. There are two reasons for processing under

Table 2.1: Vacuum phases [57]

Degree of vacuum	Pressure range	
	[Pa]	[Torr]
Rough	$10^5 > p > 10^2$	$750 > p > 7.5 \times 10^{-1}$
Fine	$10^2 > p > 10^{-1}$	$7.5 \times 10^{-1} > p > 7.5 \times 10^{-4}$
High	$10^{-1} > p > 10^{-5}$	$7.5 \times 10^{-4} > p > 7.5 \times 10^{-8}$
Ultrahigh	$10^{-5} < p$	$7.5 \times 10^{-8} < p$

(A 1 atmospheric pressure is equal to 101,325 Pascal or 760 Torr)

partial vacuum condition. The first is that it provides the atom a free path in a line-of-sigh process so that the atom can travel directly from the source to the substrate. When the atom travels, it makes collisions with gas molecules inside the process chamber. More collisions meaning that the atom will lose its energy before reaching the target substrate. The second is to minimize the contamination caused by the other gas molecules inside the process chamber. Vacuum pumps are needed to create a vacuum condition. More explaination about the vacuum pumps is described in Appendix D.

2.4 Photomask fabrication

Before doing the fabrication, the layout is transferred to photomask. Photomask is made of transparent silica glass with a pattern defined by chrome metal film. Making a photomask is almost the same process with photolithography process. The difference is that the transferring of layout design onto the chrome metal film utilizes an Electron-beam lithography (EB) machine. The process is started by dehydrate bake the blank photomask at 180 °C for 15 minutes followed by cooling for 10 minutes. Then, a selected EB tone resist is coated on the photomask' chrome metal film surface following by a soft-bake. Next, the EB machine writes the layout design on the chrome metal film surface. After that, the written photomask is developed using appropriate developers. Oxygen

Figure 2.4: Electron-beam lithography machine JBX-6300D by Jeol Ltd. *Photograph*: Clean Room, Toyohashi University of Technology

ashing process is performed after development process to make a sharp pattern of the remaining EB resist. The chrome metal film surface, which is exposed, not covered by the remaining EB resist, is etched by a ceric ammonium nitrate ($(NH_4)_2Ce(NO_3)_6$) + nitric acid (HNO_3). Finally, the remaining EB resist is removed by an SPM process. The detail of the coating recipe and the developer solution for particular EB tone resist that was used in this thesis work is shown in Table 2.2.

Table 2.2: Photomask tone resist and developer

EB positive tone resist	**EB negative tone resist**
Resist coating	
gL2700T 1st 500 rpm, 5 sec 2nd 3000 rpm, 60 sec	Primer coating using Hexamethyldisilazane (HMDS) 1st 1000 rpm, 5 sec 2nd 4000 rpm, 20 sec
	Bake (hardening), 70 °C, 3 min
	SAL601 1st 1000 rpm, 5 sec 2nd 4000 rpm, 20 sec
	Bake (hardening), 105 °C, 1 min
Developing after EB writing	
	Bake, 105 °C, 1 min
ZED-500, 40 sec	MF CD-26, 15 sec
4-methyl-2-pentanone, 10 sec	De-ionized water, 1 min
	Bake, 90 °C, 2 min

There are problems that might be occurred in the coating step. These problems apply to wafer coating and photomask coating. The first problem is the edge bead formation. For a thick resist film, there is a cumulation of resist at the edge of wafer of photomask. Especially for wafer, this edge bead may lead the wafer to stick to the photomask and induce undesired proximity-gap during exposure. The second problem is inhomogeneities. This problem comes due to the small coating area on the surface, some remaining particles on the surface, or bubbles (N_2 from the bottle that was closed for a long time, bottle is shaked, or pressing the pipette with air inside the resist) from the resist. Particles or bubbles can create a so-called comet form. To reduce the particle contamination,

blow dry with N_2 gas might help. While waiting for a while after the bottle opened, avoiding an empty pipette when getting the resist from the bottle, and adding some delays before spinning might reduce the bubbles. Figure 2.5 shows the resist inhomogeneities after resist coating on the wafer surface.

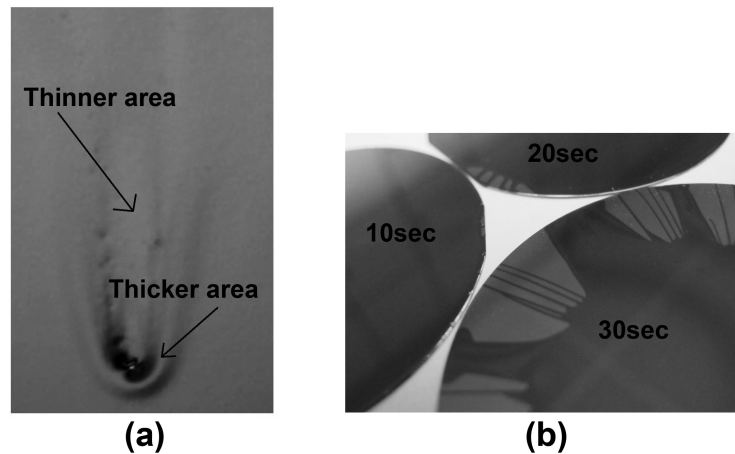


Figure 2.5: Resist inhomogeneities after spinning. (a) A comet shape caused by particles or bubbles. (b) Insufficient amount of resist and too long acceleration time. The lower wafer accelerated in 30 s, the upper one in 20 s and the left one in 10 s [58]

2.5 Deposition process

Deposition is any process to add material onto the wafer. For examples, growing the oxide as insulator, adding polysilicon as a gate, adding metals as contact or interconnect layer and coating a passivation layer to protect the underneath circuitry. The added material may come from a source material itself or a decomposed material from its compound. Physical vapor deposition (PVD) employs physical effect such as evaporate or ion bombard the liquid or solid source material into a gaseous phase to form a thin-films on the wafer. Chemical vapor deposition (CVD) adds material onto the wafer by chemical reaction of the compound materials. PVD and CVD are grouped as dry deposition process. Electrochemical or chemical deposition, spin coating, spray coating, and dip process are the example of wet deposition process. Table 2.3 shows a classification of deposition technology, mainly for thin-film deposition, from a selected literature references. [59] For fabricating the CMOS circuit in this thesis, deposition was performed for growing the oxide layer, adding polysilicon as the gate, growing the passivation layer, adding metal for contacts and interconnection layer, and coating the photoresist for photolithography process.

Table 2.3: A classification of deposition technology [59]

Evaporative methods	
* *Vacuum evaporation*	
Conventional vacuum evaporation	Molecular-beam epitaxy (MBE)
Electron-beam evaporation	Reactive evaporation
Glow-discharge processes	
* *Sputtering*	* *Plasma process*
Diode sputtering	Plasma-enhanced CVD
Reactive sputtering	Plasma oxidation
Bias sputtering (ion plating)	Plasma anodization
Magnetron sputtering	Plasma polymerization
Ion beam deposition	Plasma nitridation
Ion beam sputter	deposition Plasma reduction
Reactive ion plating	Microwave ECR plasma CVD
Cluster beam deposition (CBD)	Cathodic arc deposition
Gas-phase chemical processes	
* *Chemical Vapor Deposition (CVD)*	*Thermal Forming Processes*
CVD epitaxy	Thermal oxidation
Atmospheric-pressure CVD (APCVD)	Thermal nitridation
Low-pressure CVD (LPCVD)	Thermal polymerization
Metal-organic CVD (MOCVD)	
Photo-enhanced CVD (PHCVD)	
Laser-induced CVD (PCVD)	
Electron-enhanced CVD	Ion implantation
Liquid-phase chemical techniques	
* *Electro Processes*	*Mechanical Techniques*
Electroplating	Spary pyrolysis
Electroless plating	Spray-on techniques
Electrolytic anodization	Spin-on techniques
Chemical reduction plating	
Chemical displacement plating	
Electrophoretic deposition	Liquid phase epitaxy

2.5.1 Silicon dioxide layer deposition

A thermal oxidation furnace was used to grow the silicon dioxide (SiO_2) layer. The SiO_2 was utilized as sacrifice-oxide before (using dry oxidation) ion implantation process to protect the silicon surface from the damages and as field oxidation layer (using wet oxidation) to raise the threshold voltage outside the transistor areas. Figure 2.6 shows the simplify diagram of a thermal oxidation furnace and Figure 2.7 shows the oxidation furnace. Dry oxidation has a lower growth rate but produce high quality of oxide layer. Meanwhile, wet oxidation growths the oxide layer

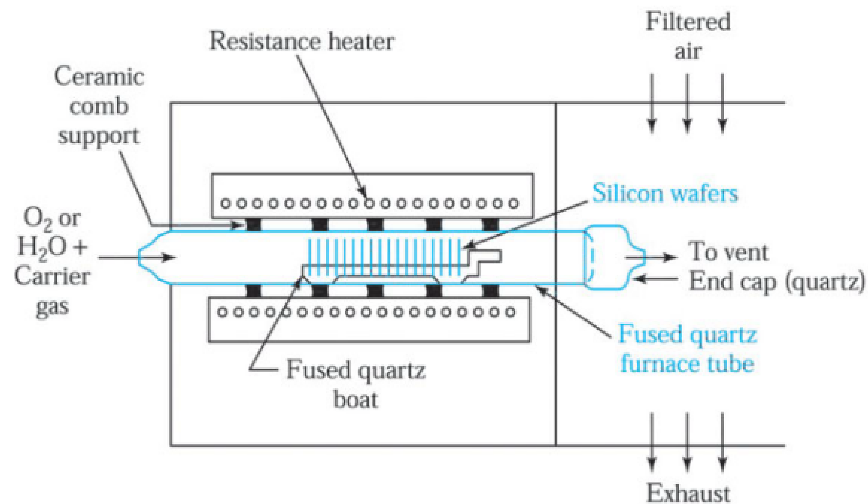


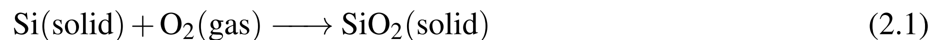
Figure 2.6: Schematic of the thermal oxidation furnace for dry and wet processing [60]

faster but has low quality of oxide layer due to the water content. The steps to make up the furnace thermal oxidation process are:

1. Preparing the furnace (checking the gases flow, setting the temperature, etc.)
2. Loading the RCA-cleaned wafer onto the quartz boat. It is important to keep the wafer clean from contaminations until the oxidation process begins. The main wafers are placed in between the dummy wafers to keep the uniformity. A reference wafers also should be added to check the thickness of the oxide layer.
3. Loading the quartz boat into the quartz tube very slowly (approximately 1 cm/s).
4. After the temperature is stable, starting the process by changing the dummy gas (N_2) with O_2 only for dry process or O_2 followed by H_2 for wet process. In wet process, making sure that the water vapor is formed by bringing a glass near to the gasses outlet and checking whether a steam or a mist can be seen.
5. Unloading the quartz boat from the quartz tube.
6. Measuring the thickness of the oxide layer.
7. Shutting down the furnace and saving the wafers for the next process.

The chemical reactions inside the oxidation furnace for dry oxidation and wet oxidation are shown in eq. 2.1 and eq. 2.2, respectively.

Figure 2.7: Oxidation furnace. (top) Six furnaces for different use and temperature. (bottom) Wafers are loaded in the quartz boat. *Photograph*: Clean Room, Toyohashi University of Technology



$$\mathrm{Si(solid)} + \mathrm{O_2(gas)} \longrightarrow \mathrm{SiO_2(solid)} \tag{2.1}$$

$$\mathrm{Si(solid)} + 2\,\mathrm{H_2O\,(gas)} \longrightarrow \mathrm{SiO_2(solid)} + 2\,\mathrm{H_2(gas)} \tag{2.2}$$

When depositing silicon dioxide on the silicon, the silicon will be consumed about 44% of the total silicon dioxide thickness. [60] Meaning that, if a 100 nm of silicon dioxide was growth then a layer of 44 nm of silicon was consumed. Figure 2.8 shows the experimental resuls of the silicon dioxide as a function of oxidation time and temperature for two substrate orientation. At the same condition, silicon dioxide grows faster on polysilicon comparing to silicon. For example, when growing the silicon dioxide for protection layer on polysilicon, the silicon dioxide thickness on the reference wafer which is a bare silicon was 58 nm. Meanwhile the silicon dioxide thickness on the samples which had polysilicon layer was 66 nm. The environment was using furnace number 4, 1000 °C of temperature, 250 L/h of oxygen flow for 10 minutes, and 10 minutes purged with nitrogen gas.

Before forming the contacts and metalization, a passivation layer was growth using LP-CVD process. LP-CVD works at a pressure range of 10 - 1,000 Pa. Reducing the pressure is intended to reduce unwanted gas-phase reactions because the ratio of the mass transport velocity, hence decreasing the diffusion of the gas. As the result, it improves the uniformity on the wafer. The

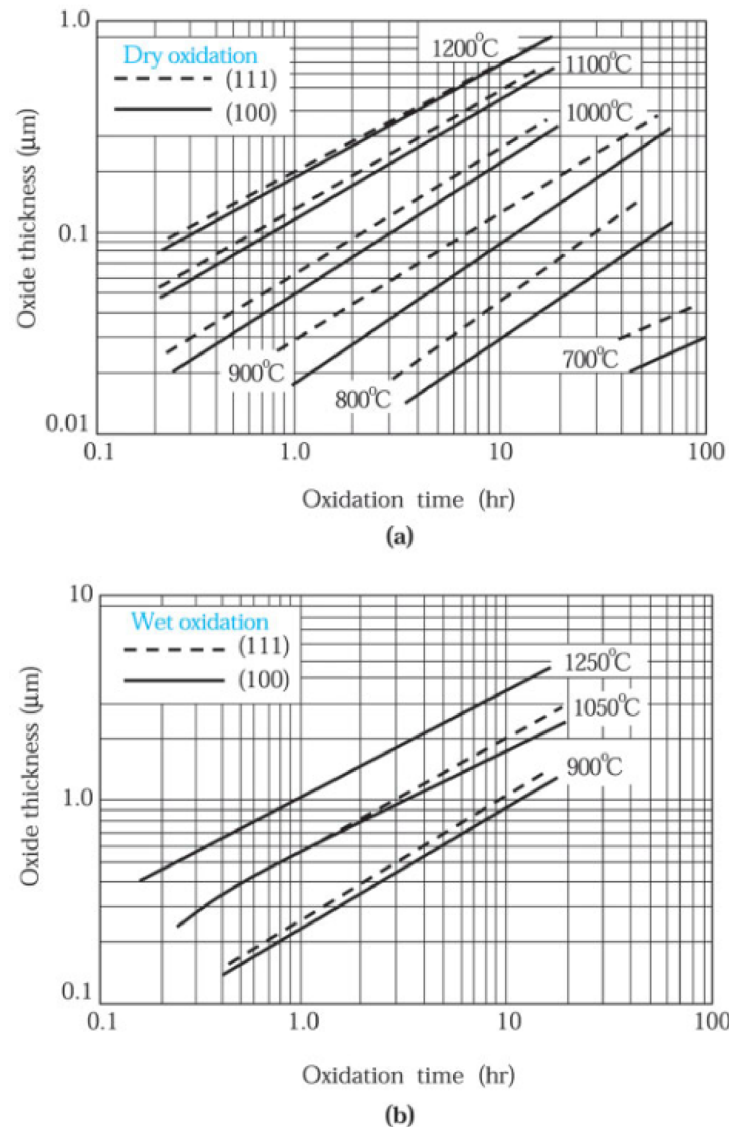


Figure 2.8: Graphs of experimental results of silicon dioxide thickness by varying the time and the temperature for two substrate orientation. (a) For dry oxidation. (b) For wet oxidation [60]

gases sources for the oxide layer are tetra ethyl ortho silicate (TEOS, $Si(OC_2H_5)_4$) and the oxygen which are deposited between 650 - 750 °C. The TEOS and the oxygen produces SiO_2 solid which deposited on the silicon wafer surface, H_2O gas, and CO_2 gas, where the gases products are pumped out. Figure 2.9 shows the diagram of LP-CVD furnace for depositing oxide layer with TEOS.

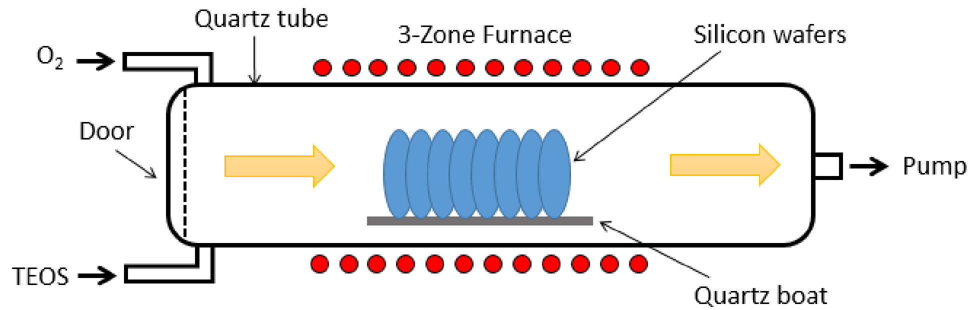


Figure 2.9: LP-CVD with TEOS source for depositing oxide layer

2.5.2 Polysilicon deposition

The polysilicon was also grown by using LP-CVD. The gasses source are silane (SiH_4) and nitrogen. The temperature and the pressure are 620 °C and 67 Pa, respectively. The chemical reaction is shown in eq. 2.3.

$$SiH_4 \xrightarrow{620\,^{\circ}C} Si + 2\,H_2 \tag{2.3}$$

As well as in depositing silicon dioxide, when depositing polysilicon, dummy wafers are placed at the front side and the back side. Reference wafers are also placed along with the main wafers. The backside of the wafers is facing the gas flow direction in the tube of the furnace. Figure 2.10 shows the placement of the wafers during deposition process. After the process is finished, the reference wafer is checked for the thickness. Checking the thickness of polysilicon on the silicon wafer is impossible because they have the same refractive index. To addressing this problem, the reference wafer should be included in the previous process, i.e. the gate oxidation. By using this method, the polysilicon thickness can be measured.

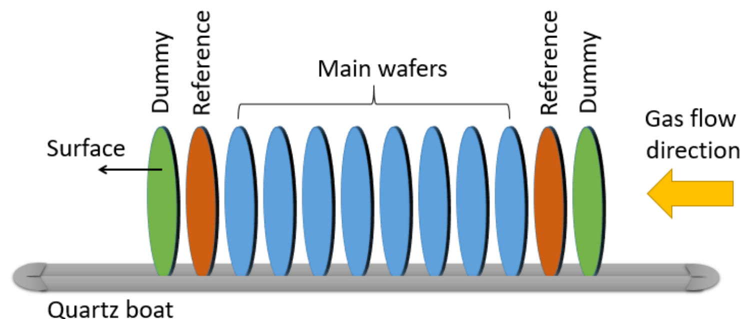


Figure 2.10: Wafer placement during deposition.

2.5.3 Metal deposition

For the metal deposition, a DC magnetron sputtering was used. In vacuum thermal evaporation method, the target source atoms are evaporated by using resistance heating or electron beam heating. The evaporation with electron beam heating allows depositing materials with a high melting point (such as W, Ta, and C). In contrast, sputtering deposition exploits the interaction of ions (usually the inert gases ions, such as Argon) to knock-on the target source. The Ar ions may make up a series of collisions between the atoms of the target source, then it possibly ejects some of the atoms of the target source which move towards and deposit on the silicon wafer surface. The DC sputtering is used for conductive targets, while the RF sputtering can be used for insulator targets also. The magnetron sputtering increases the number of Ar ions by trapping the electrons which are produced when the ions hit the target source near the target source. The trapped electrons follow the helical paths around the magnetic field and hit the Ar atoms to generate more Ar ions. Since the ejected target source's atoms are neutrally charged, they do not affected by the magnetic field. As the result, magnetron sputtering has a high deposition rate, reducing the bombardment of the silicon wafer hence lowering the deposition temperature, and can be operated at lower pressure. Figure 2.11 describes the sputtering physic and sputtering process.

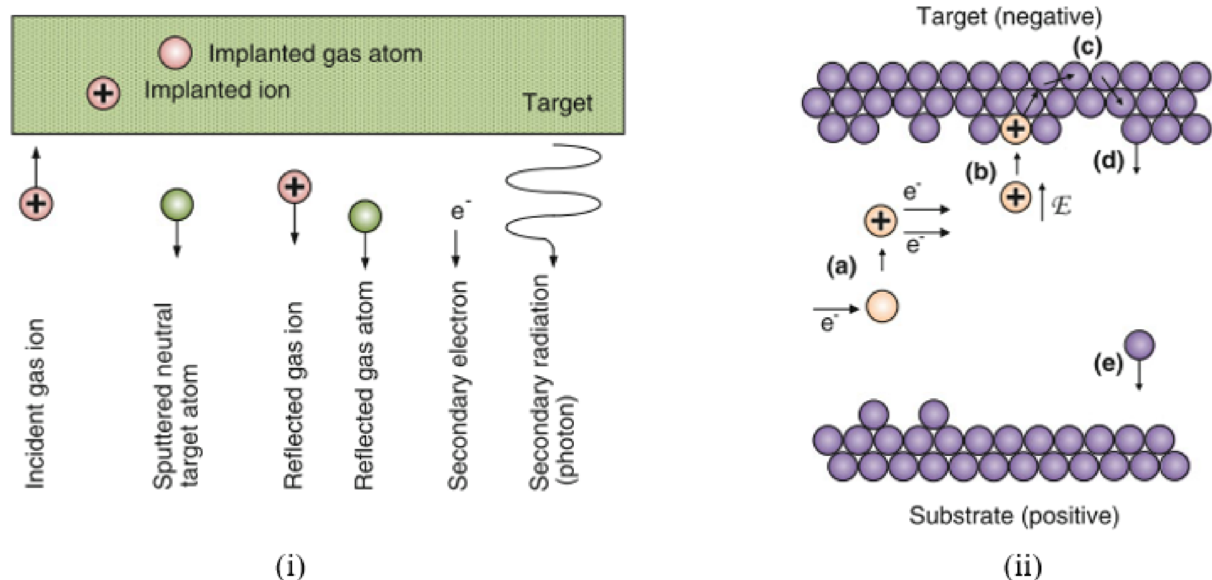


Figure 2.11: Sputtering interaction. (i) Occuring dominant effects in a target bombardment. (ii) Sputtering process: (a) Ionizing of a sputter gas atom. (b) Ion's acceleration towards the target source and impact. (c) A series collision at the target source's surface. (d) Ejection (sputtering) of a target atom. (e) Sputtered atom move towards the substrate [57]

Aluminum alloyed with silicon was used for metalization in this thesis work. It has low resistivity and satisfy the low-resistance requirements. The resistivity of aluminum is 2.7 $\mu\Omega$-cm, while its alloy may up to 3.5 $\mu\Omega$-cm. There is a problem so called junction spiking. In the circuit, Al makes a contact with the silicon at the source and drain area. Pure Al melts at 660 °C and pure silicon melts at 1412 °C. But in Al-Si system introduces eutectic feature, it tells that the addition of other metal lowers the melting point of the system. Due to this eutectic feature, above 577 °C the system will melt. So, after depositing a pure Al, if the system is heating up, at the interface of Al-Si, the silicon will diffuse into the Al and vice versa. Then, when more silicon atoms is sucked up into the Al, an empty space is created at the location where the silicon atoms have moved. Finally, the Al fills up the empty space. As the result, the pn-junction will be short-circuited by the Al. To overcome this problem, silicon is added into the Al. By doing so, the Al will not suck up the silicon when the system is heating up. Using alloyed of 0.5% - 1% of silicon is enough to avoid the spiking problem. In this thesis work, the metalization is used an AlSi with a composition of 99% of Al and 1% of Si. Another technique to avoid the junction spiking is by depositing a barrier metal layer before the Al. Titanium Nitride (TiN) is generally used because it satisfied the requirements, i.e. has low contact resistance with silicon, no reaction with the Al, and compatible with the rest processes. Figure 2.12 shows the aluminum metalization spiking in the silicon and the inserted barrier metal layer.

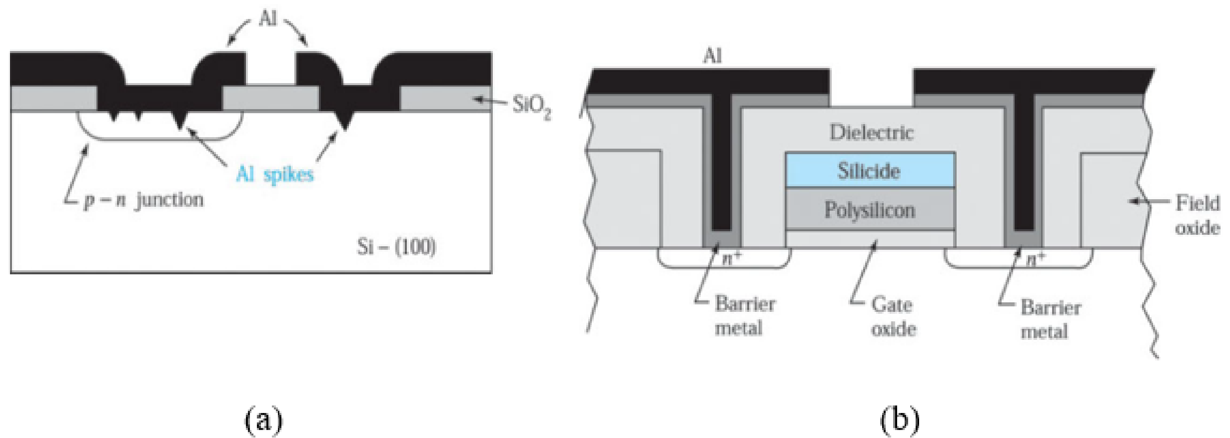


Figure 2.12: Aluminum metalization. (a) The aluminum spiking in the silicon. (b) Barrier metal between aluminum and silicon [60]

2.5.4 Photoresist deposition

In the photolithography process, a photoresist was deposited on the surface of the silicon wafer. For this purpose, a spin-coater was used. When performing a spin-coating, the silicon wafer is held by a vacuum chuck and previously has a treatment to enhance the adhesion. Figure 2.13 shows the spin-coating process steps to deposit the photoresist. The time delay step after the dispensing the photoresist has a function to allow the photoresist for spreading, or performed by slow spin with a rotation velocity around 500 rpm (rotation per minute). At the rotation step, the spin velocity is rising to 2,000 - 4,000 rpm. Figure 2.14 shows the spin-coater that we used in our laboratory.

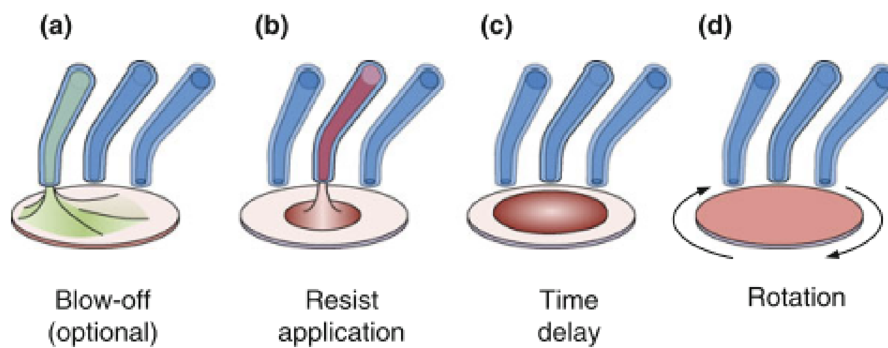


Figure 2.13: The process of spin-coating. (a) Blow-off (optional). (b) Photoresist application. (c) Time delay to allow spreading. (d) Spinning [57]

Figure 2.14: Suss Delta80 spin-coater with hotplate. *Photograph*: Clean Room, Toyohashi University of Technology

2.6 Removal process

Removal is any process to remove unwanted material from the wafer. In this section, related to this thesis work, etching, peeling, and cleaning are categorized as removal. Etching process refers to removing a layer under a patterned photoresist from the wafer, stripping or peeling process indicates as removing the photoresist after etching process, and cleaning means removing the contaminants from the wafer surface before a process begins.

2.6.1 Materials etching

After development process in the photolithography process (explained in section 2.5), the weak part of the photoresist is removed, exposing the layer beneath. Then, the layer under the patterned photoresist is ready to be etched. The material etching process can be classified by two criteria: etch profile and etchan types. Figure 2.15 and Figure 2.16 shows the illustration process of etching profile and the main advantages between wet and dry etching, respectively. The etching type that was used to process the CMOS circuit in this thesis work is shown in Table 2.4.

The etch profile criterion are described as follows:

- Selectivity etch: etching one layer in a multilayer structure by using an etchan that has different etching rate ratio for different layers. A good selectivity etch removes one layer completely without etches the other layers. This profile is mostly used in Microelectromechanical system (MEMS).
- Isotropy etch: in a masked structure (the mask was formed by the photoresist), the underneath layer is etched by the same direction vertically and horizontally creating undercut. The undercut distance is called as bias.

Figure 2.15: Illustration of the etching profile

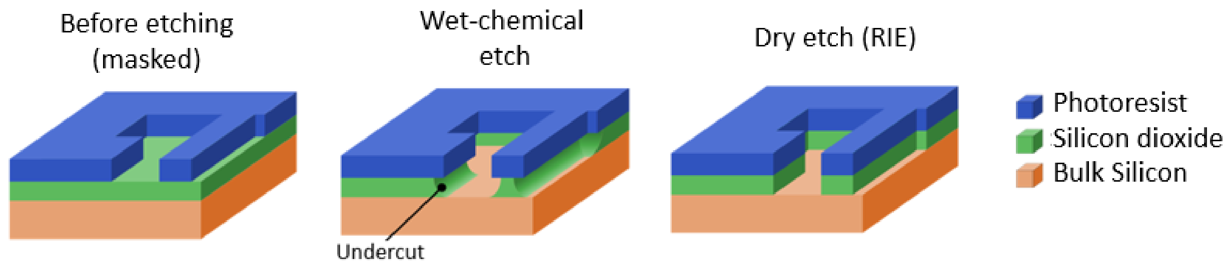


Figure 2.16: The result of wet and dry etching. (*Image was modified from https://de.wikipedia.org/wiki/Trockenätzen*)

Table 2.4: Selected etching process

Material to be etched	Process	Etchan
Silicon for alignment mark	Dry etching (RIE)	SF_6
Silicon dioxide (sac, FOX)	Wet etching	BHF16
Polysilicon for gate	Dry etching (ICP-RIE)	SF_6/O_2
Aluminum for interconnection	Wet etching	H_3PO_4 + HNO_3 + H_2O

- Anisotropy etch: in a masked structure, the etchan etches at different rate depending on the crystalline orientation which makes the etching ratio between vertical direction and horizontal direction differs.
- Directional etch: in a masked structure, the ions bombard create a vertical direction etch. This profile utilizes dry etching process.

The etchan types are described as follows:

- Wet etching: a liquid-phase (wet) etchan is used. Different material etching requires different etchan solutions. Wet etching result is isotropic but using other etchans such as Ethylenediamine pyrocatechol (EDP), Potassium hydroxide/Isopropyl alcohol (KOH/IPA), and Tetramethylammonium hydroxide (TMAH), the result is anisotropic.
- Dry/Plasma etching: a plasma-phase (dry) etchan is used. The plasma is operating in vacuum environment. The plasma generates free radicals that reacts with the material to be etched then produces products to be removed.

2.6.2 Photoresist stripping

After patterning and material etching, the task of the photoresist is completed, therefore the photoresist can be removed. Stripping the photoresist can be done by wet or dry process. In wet process, the photoresist is removed by dipping in the boiled at 120 °C of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) mixture (SPM) solution for 5 - 10 minutes. While in the dry process, a plasma of oxygen gas reacts with the photoresist to produce CO, CO_2, and water vapor which are sucked out from the vacuum chamber, so that the process is called ashing process.

2.6.3 Wafer cleaning

Before processing especially for oxidation step, the wafer should be clean to minimize the contaminant on the wafer's surface. The contaminant might be particles, organic (photoresist), metals, and surface oxide layer. In this thesis work, the common used wafer cleaning process is shown in Table 2.5, which follows the RCA standard which developed by Werner Kern while working for Radio Corporation of America (RCA) in 1965. APM stands for ammonia peroxide mixture, HPM stands for hydrogen peroxide mixture, and SPM stands for sulfuric peroxide mixture.

In those RCA cleaning processes, APM, HPM, and SPM processes use glass beakers because the solutions need to be boiled and Teflon-based materials for handling the wafer. Meanwhile, DHF and BHF16 processes might etch the glass, then non-glass tools should be used, such as plastic beaker and Teflon-based materials.

Handling the wafer during the process is also important. The wafer should be held using different tweezers for different purposes. In the photolithography step, the tweezer might contaminate with the photoresist, hence it should not be used for other processes. During the wafer cleaning process, dipping a metal tweezer into the solution should be avoided because the metal might dissolves and contaminates the wafer through the solution. One can use a Teflon-based tweezer in this case. During oxide and polysilicon depositions, different tweezers also should be used. After cleaning, spin dryer can be used to dry the wafer but a care must be taken when loading and unloading the wafers because particle contamination might happen. Figure 2.17 shows the spin dryer used in our facilities.

Considering that the solutions might cause a hazard for human, safety wearing such as safety-glasses, chemical-resistance apron, and heat and chemical resistance gloves must be worn during the process.

Table 2.5: Wafer cleaning process

Process name	**Conditions**	**Target of removal**	**Side effects**	**pH**	**Surface oxide**
SC-1 (APM)	NH_4OH:H_2O_2:H_2O = 1:1:5 70-80 °C, 10 min	Particles, Organics	Metal contamination	10-12	created
SC-2 (HPM)	HCl:H_2O_2:H_2O = 1:1:6 70-80 °C, 10 min	Metal	Particle absorption	0-2	created
SPM	H_2SO_4:H_2O_2 = 3:1 100-120 °C, 10 min	Organics, Metal	Particle absorption	0-2	created
Diluted HF (DHF)	HF:H_2O = 1:50	Surface oxide, Metals (except for Cu)	Particle absorption, Cu deposition (CuF_2)	0-2	removed
Buffered HF (BHF16)	HF:NH_4F = 7:1	Surface oxide	Particle absorption, Cu deposition	0-2	removed

Figure 2.17: A spin dryer while operating for 2 inch wafers. *Photograph*: Clean Room, Toyohashi University of Technology

2.7 Patterning process

Patterning is a process to change the shape of the deposited material. It commonly refers as lithography or photolithography. Photolithography is the most important process in the IC fabrication. It consumes 40-50% of total wafer process time and it determines the minimum feature size of the transistor. This process temporarily coats the photoresist on the wafer to transfer the design pattern to the photoresist. Photoresist is a photo sensitive material which is sensitive to ultraviolet light. That is why the photolithography process is performed in the room with yellow illumination which is called as a yellow room. The basic steps in the photolithography is shown in Table 2.6.

Table 2.6: Photolithography process

Step name	**Equipment & Conditions**	**Purpose**
	Photoresist coating	
Dehydrate bake	Hot plate, 160 °C, 5 min	Remove moisture, increase photoresist adhesive
Photoresist coating	Spin coater	Coating the photoresist
Pre-bake	Hot plate, 110 °C, 90 sec	Soft-bake, hardening the photoresist
	Alignment & Exposure	
Alignment & Exposure	Suss aligner, exposure time 4 sec at 3.15 $\mu W/cm^2$	Transferring the design pattern from the photomask to the photoresist
	Development	
Development	Drafter, developer and rinse solutions	Remove the weak photoresist
Drying	Dry nitrogen blow	Dry the wafer from solutions
Inspection	Microscope	Pattern inspection, if fail then remove the photoresist and restart the process
Post-bake	Hot plate, 140 °C for negative resist or 160 °C for positive resist, 5 min	Hard-bake, hardening the remaining photoresist after development

There are two types of photoresist: negative and positive. Figure 2.18 shows the comparison between a negative photoresist and a positive photoresist. In this thesis work, a negative photoresist of OMR100-40cP was used which widely uses in 1970 but has a poor resolution at 5μm. A positive photoresist of OFPR8600 52-cP was used which has a high resolution at 0.1μm. Primer coating is needed before positive photoresist type to increase the adhesiveness of photoresist to the wafer's surface. Each type of photoresists has different treatment and different developer solution, as shown in Table 2.7 for silicon wafers.

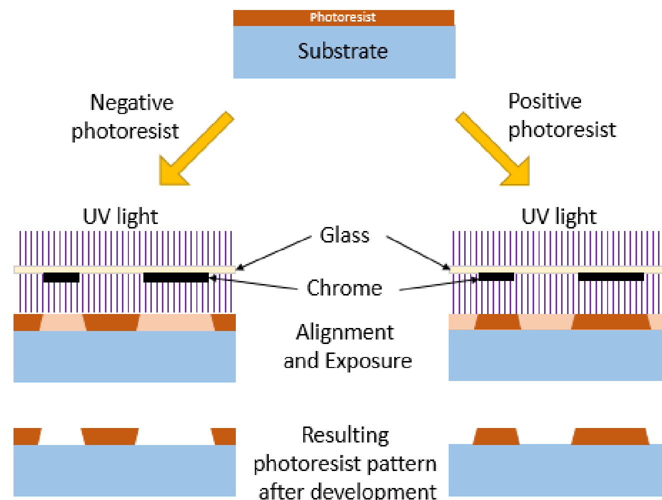


Figure 2.18: Comparison between a negative photoresist and a positive photoresist

Photoresist is composed of polymer, solvents, sensitizers, and additives. Polymer is a solid organic material that changes solubility due to photochemical reaction when exposed to UV light. Solvent dissolves the polymer into liquid and occupies 75% portion of the photoresist. Sensitizers control and/or modifies photochemical reaction of photoresist during exposure, hence determine exposure time and intensity. Additives are various added chemical to obtain desired process result, such as dyes to reduce reflection. Dehydrate bake is useful to remove the moisture from the wafer's surface and increasing the adhesiveness between photoresist and the wafer's surface. Pre-bake, also known as soft-bake, evaporates almost 80% solvent in the photoresist and makes a smooth photoresist sidewall hence improving the resolution. Post-bake, also known as hard-bake, evaporates all solvents in the photoresist, improves photoresist adhesion with wafer's surface, polymerizes and stabilizes the photoresist, and makes the photoresist flow to fill any pinholes.

Karl Suss Mask Aligner MA/BA6 from Suss Microtec, as shown in Figure 2.19, was used for the aligner and exposure. For this purpose, some parameters setting are exposure at 4 seconds, gap at 50 μm, type of contact at soft/contact, and top side alignment (TSA) method.

Table 2.7: Photoresist coating and developer solution

Step	**Conditions**
Positive photoresist coating steps	
Primer coating using Hexamethyldisilazane (HMDS)	1st 1000 rpm, 5 sec 2nd 4000 rpm, 20 sec
Positive resist OFPR8600 52-cP	1st 1000 rpm, 5 sec 2nd 4000 rpm, 20 sec
Positive photoresist development steps	
NMD-3 developer	Room temperature, 23 sec
Deionized water overflow	60 sec
Negative photoresist coating steps	
Negative resist OMR100 40-cP	1st 500 rpm, 5 sec 2nd 4000 rpm, 20 sec
Negative photoresist development steps	
OMR SL developer	Room temperature, 120 sec
OMR rinse	120 sec

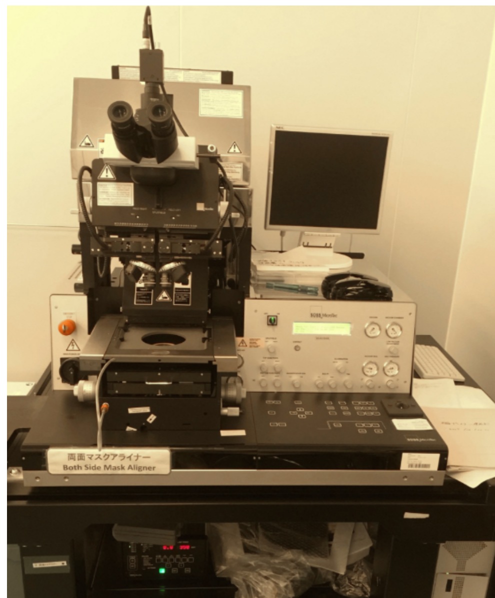


Figure 2.19: Suss aligner. *Photograph*: Clean Room, Toyohashi University of Technology

2.8 Modification of electrical properties

This process is referred as doping process. Impurity atoms are inserted into the silicon wafer, either by diffusion or ion implantation, to create a selected N-type or P-type region. Ion implantation shots the silicon wafer with the impurity atoms at a high energy. This may damage the silicon bonds. Annealing is a treatment to repair the damage after ion implantation process by heating the wafer at a high temperature. In this thesis work, the CMOS circuit fabrication used an ion implantation process.

Figure 2.20 (a) shows the diagram of the ion implanter. [57] The ion source and extraction optics of enhanced Bernas type is shown in Figure 2.20 (b). In the arc chamber, a filament made of tungsten is resistively heated as a cathode. The arc potential between the filament and the arc chamber makes the electrons are released from the filament. The repellent in front of the filaments has a negative charged and reserves the direction of the electrons back to the cathode. An added magnetic field B causes the electrons move in spiral to maximize the collision between electrons and dopant gas which is entering the arc chamber through the small hole. Therefore, a plasma occurs in the arc chamber. The ionized dopants leave the arc chamber through a slit-opening called the arc slit. Next to the arc slit, there are a pair of slit electrode. The nearest electrodes are suppression electrode, repeals the back-streaming electrons and also prevents surplus X-ray generation since the electrodes are negatively charged. The outer electrodes are grounded to extract and accelerate ions from the arc chamber to the beamline.

Next, to choose the correct species of the ion source charge, a magnetic field is used to bend the trajectory of the ions and the desired ones will go through the mass resolving slit. These desired ions are accelerated or decelerated by a DC potential. Then the beam scanning implants the ions to the wafer. The scanning process might be moving the wafer relative to the beam, moving the beam relative to the wafer, or both. Controlling the uniformity of implantation process is important. Before and during implantation, the system checks the uniformity by detecting the received intensity in the implantation area. If an area receives more intensity then later the scanning speed will be increased for that area, and vice versa.

During the bombardment, wafer surface may generate a positive charge. This positive charge may cause a current flow to the sensitive components. To avoid this problem, the ion implantation system equips with a compensating electron current flow to the wafer surface which is typically used a plasma flood system.

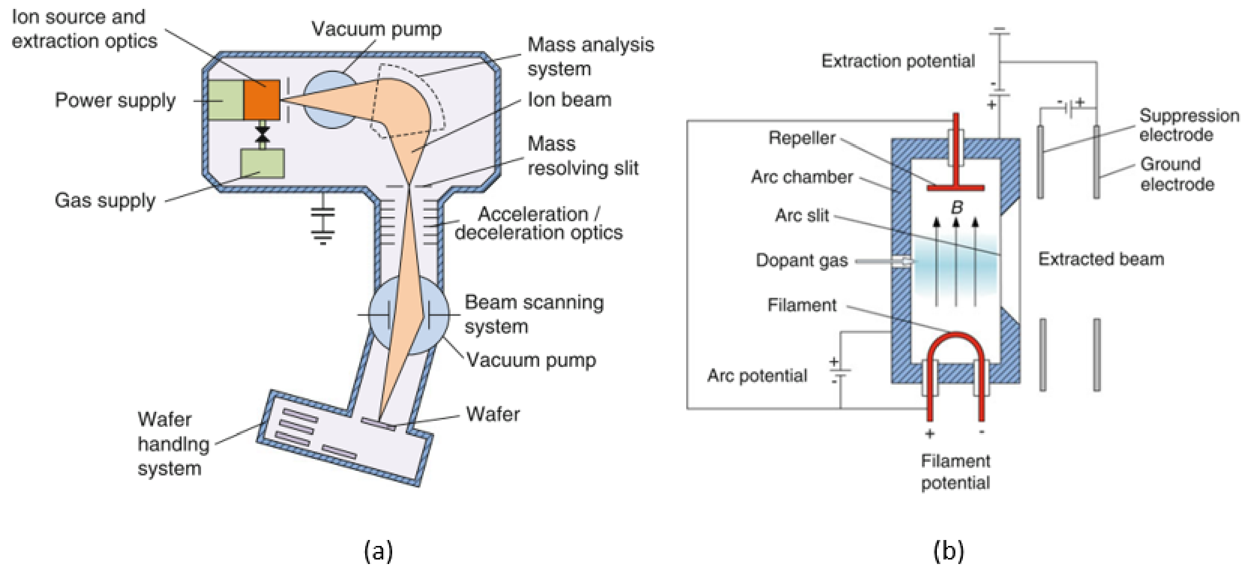


Figure 2.20: Ion implanter diagram. (a) Diagram of ion implanter. (b) Ion source and extraction optics [57]

Figure 2.21: Ion implantation system EXCEED2300/2300H. *Photograph*: Clean Room, Toyohashi University of Technology

The wafer handling system (the end station) has a duty providing the ion implantation system with a continuous flows of wafers. It has an arm robots. Starting by picking the wafer from the factory cassette, searching the wafer flat or notch and facing it to an appropriate direction, moving the wafer to the implant chamber, returning the implanted wafer from the implant chamber to the factory cassette, and repeating the process for the remaining unimplanted wafer. Figure 2.21 shows the ion implanter that was used in this thesis work which occupied an area of 3.2 x 6.5 m^2.

After the device fabrication has been completed, usually it continues with several measurements of device characteristics including I-V curves, C-V curves, response time, or other functional tests in the wafer or chip level. Then, it continues with dicing process. Finally, the dies are packaged. Device fabrication is performed in an environment with controlled contaminant, so called cleanroom or clean room. Appendix E briefly introduces about the cleanroom.

2.9 Conclusion

Fabricating a CMOS circuit needs a repeating process, as shown in Figure 2.22. As an example, to make a N-well from a fresh wafer, the first is, removing the contaminant on the surface of the wafer, it is also called as cleaning. The second is, depositing a thin oxide film on the wafer's surface to protect the surface from the next process. The third is, patterning the N-well area. The fourth is, implanting the Phosphorus ions. Finally, removing the patterned resist. Then, to create another structure such as P-well formation, the processes are repeated.

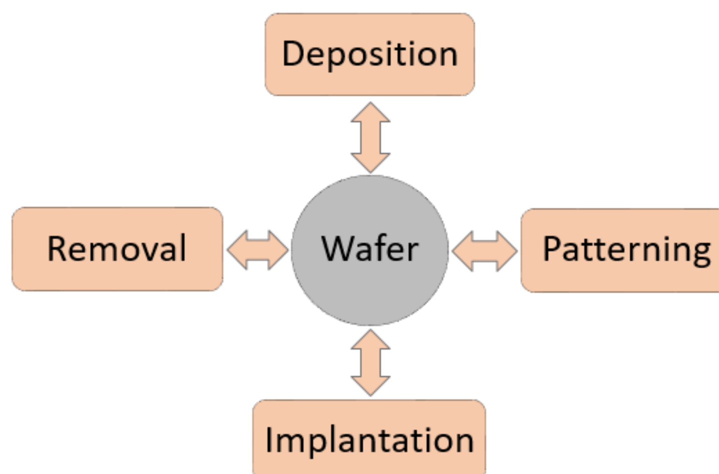


Figure 2.22: Device fabrication process flow

In this chapter, a brief introduction about the aims of each equipment was described along with the author's experiences during fabrication processes. Knowing the basic principles of the material physics and equipments is also important. Considering that the equipments are not easy to operate and the materials are dangerous to human when cares are not taken. Standard operation procedures, manuals, and safety prevention system must be provided. By decreasing the feature size nowadays, new physical phenomenas might occur, hence the fabrication tools are more advanced to meet the requirements.

Chapter 3

A biological-inspired edge detection circuit as the neuro-OEIC

3.1 Introduction

The image data from the focal plane array is pre-processed before the image data is sent to the main processing unit (the FPGA). Since the inner area of the object which represents a hydrogen flame within the image data can be neglected, an edge detection circuit is needed to obtain the perimeter of the object. Bringing the edge detection circuit into the main processing unit is possible, but it was preferred to use analog circuit to implement the edge detection circuit because of its simplicity and fast execution time comparing to digital circuit implementation. A biological-inspired edge detection circuit that mimics the outer vertebrate retina developed by Kimihiro Nishio was a candidate to be implemented in this thesis work. Since the AlGaN based on sapphire focal plane array will be integrated with this biological-inspired edge detection circuit, we called this integration as a neuro-OEIC. This chapter describes about the analog edge detection circuit which mimics the outer vertebrate retina, simulates the circuit in one-dimensional and two-dimensional array, presents the experimental results and discussion, and finally concludes discusses about the further development.

3.2 Silicon diode readout circuit design

There are two methods of converting the photocurrent generated by the photodiode into a voltage using a short-circuit current as shown in Figure 3.1. In this research work, the readout circuit was configured as Figure 3.1(b). Comparing to Figure 3.1(a), the readout circuit allows the photocurrent to flow continuously and the converted result can be read at any time. Another advantage is that the photocurrent is logarithmic compressed, hence a wide dynamic range of the radiation power received by the photodiode can be obtained.

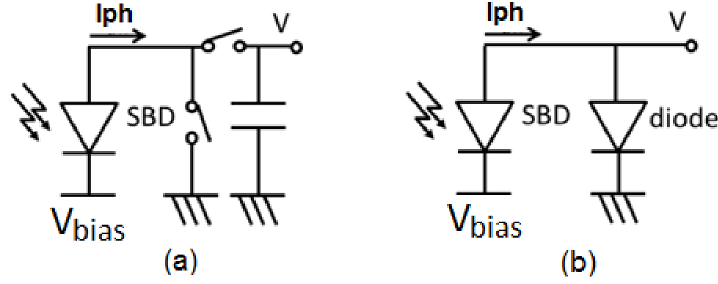


Figure 3.1: The voltage conversion method using a short-circuit current. [37] (a) Charge-voltage converter (linear). (b) Current-voltage converter (logarithmic)

The open circuit voltage at the silicon diode is expressed by eq. 3.1,

$$V_O = \frac{k.T}{q} ln\left(1 + \frac{I_{PH}}{I_S}\right) \tag{3.1}$$

where k is the Boltzmann's constant (=1.38 $\times 10^{-23}$ J/K), T is the absolute temperature in Kelvin, q is the elementary charge, I_{PH} is the photocurrent which flows to the silicon diode, and I_S is the reverse saturation current of the silicon diode which can be calculated as in eq. 3.2.

$$I_S = J_S.A_j = q\left(\frac{D_p.p_{n0}}{L_p} + \frac{D_n.n_{p0}}{L_n}\right).A_j \tag{3.2}$$

where J_S is the current density, A_j is the cross sectional area, q is the elementary charge, D is the diffusion coefficient, p_{n0} is the minority carrier concentration in the n-type semiconductor, n_{p0} is the minority carrier concentration in the p-type semiconductor, and L is the diffusion length for each density. The index p denotes the holes and the index n denotes the electrons.

The diffusion length (L) can be calculated from the diffusion coefficient (D) and recombination time (τ) as in eq. 3.3.

$$\begin{aligned} L_p &= \sqrt{D_p \tau_p} \\ L_n &= \sqrt{D_n \tau_n} \end{aligned} \tag{3.3}$$

The minority carrier concentrations are calculated using the number of donor (N_A) or acceptor (N_D) concentration and the number of the intrinsic carrier concentration (n_i) as in eq. 3.4. For silicon, the intrinsic carrier concentration is 1.5 $\times 10^{10}$ cm^3 at temperature of 300 K.

$$
\begin{aligned}
p_{n0} &= \frac{n_i^2}{N_A} \\
n_{p0} &= \frac{n_i^2}{N_D}
\end{aligned} \tag{3.4}
$$

By substituting eq. 3.3 and eq. 3.4 into eq. 3.2, then eq. 3.5 can be obtained.

$$
I_S = J_S.A_j = A_j.q.n_i^2\left(\frac{1}{N_A}.\sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_D}.\sqrt{\frac{D_n}{\tau_n}}\right). \tag{3.5}
$$

The diffusion coefficient (D) also can be given in term of electron mobilities (μ_n) and hole mobilities (μ_p) as in eq. 3.6.

$$
\begin{aligned}
D_n &= \frac{kT}{q}\mu_n \\
D_p &= \frac{kT}{q}\mu_p
\end{aligned} \tag{3.6}
$$

In this thesis work, the silicon diode is fabricated along with the MOS transistors. Figure 3.2 shows the silicon diode design. The silicon diode is built using P-active contact in the N-well as the anode and surrounding with N-Well contact as the cathode. The size of the active area of the anode is 50 μm $\times$ 50 μm. It is assumed that the diode current will flow only in vertical direction from the anode to the cathode through the N-well with no side-wall current flowing. In this case, the

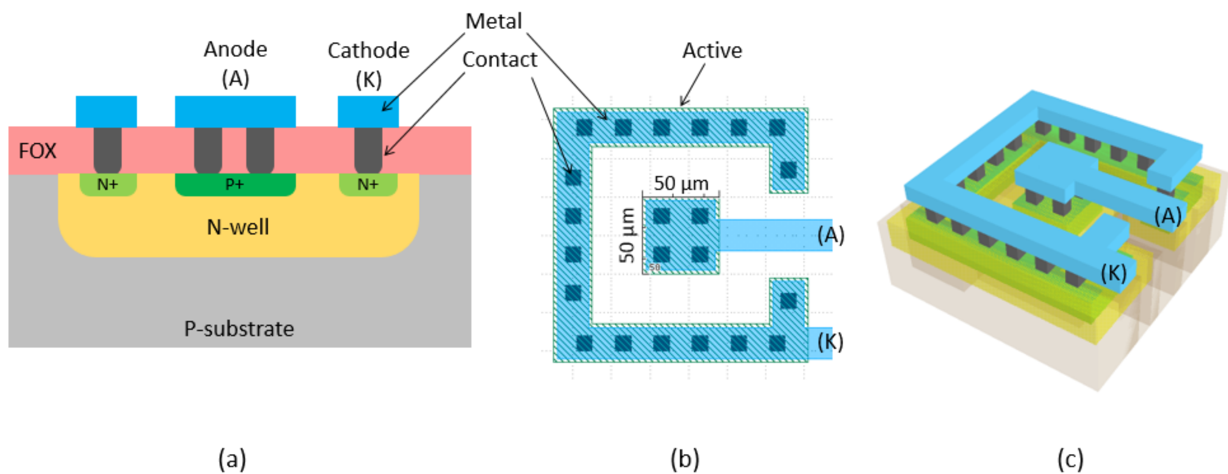


Figure 3.2: The silicon diode design. (a) Cross sectional design. (b) Layout design. (c) Layout in 3D view

parameter A_j is (50 μm $\times$ 50 μm =) 2500 μm^2. The cathode of the silicon diode, which formed from an N-well, was made with the same process as the N-well of the PMOS transistors. The anode of the silicon diode, which made from a P-active, was also fabricated with the same process as the source/drain of the PMOS transistors.

The N-well process was ion implanted by phosphorus ions at a dose of 5×10^{12} cm^{-2} with an acceleration energy of 150 KeV, followed with annealing at temperature of 1150 °C for 9 hours. This gives the number of donor (N_D) of 1.193×10^{16} cm^{-3} at the surface. Meanwhile, the P-active was ion implanted by boron ions at a dose of 4×10^{15} cm^2 with an acceleration energy of 30 KeV, followed with annealing at temperature of 900 °C for 20 minutes. Thus, the number of acceptor (N_A) was 2.02×10^{19} cm^3 at the surface. Those values gives the photodiode to generate a reserve saturation current of 1.53×10^{-13} A.

Figure 3.3 shows the simulation using SPICE when the generated photocurrent flows through the designed silicon diode. The minimum of the expected photocurrent of 14.1 fA produces a voltage drop of 1.97 mV, while the maximum of the expected photocurrent of 14.1 nA gives a voltage drop of 295.67 mV. It clearly shows that the silicon diode can compress the six order at the input into two order at the output. Table 3.1 shows the resume of the range of the radiation power to the voltage drop on the silicon diode.

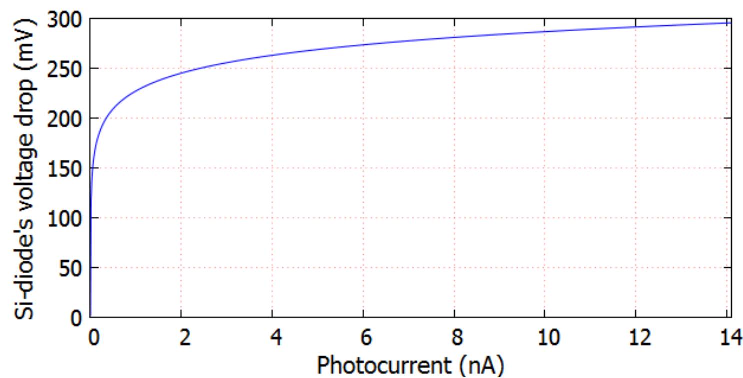


Figure 3.3: Simulation result of voltage drop on the silicon diode

Table 3.1: Silicon diode voltage drop at given radiation power

Radiation power	Photocurrent	Silicon diode voltage drop
10 pW/mm^2 (minimum)	14.1 fA	1.97 mV
10 μW/mm^2 (maximum)	14.1 nA	295.67 mV

3.3 Outer vertebrate retina edge detection circuit

As shown in Figure 3.4, a vertebrate retina has many different layers [61]. The outer retina consists of photoreceptor (photodetector) cells, horizontal cells, and bipolar cells. While the inner retina consists of amacrin cells, ganglion cells, and optical nerves. The detail of their function is not discussed in this work. The outer retina is not only doing the light sensing, but also pre-processing the received images. The outer retina is capable to get an edge information from the received images. The model of the outer vertebrate retina, which explains how the outer vertebrate retina works, is shown in Figure 3.5.

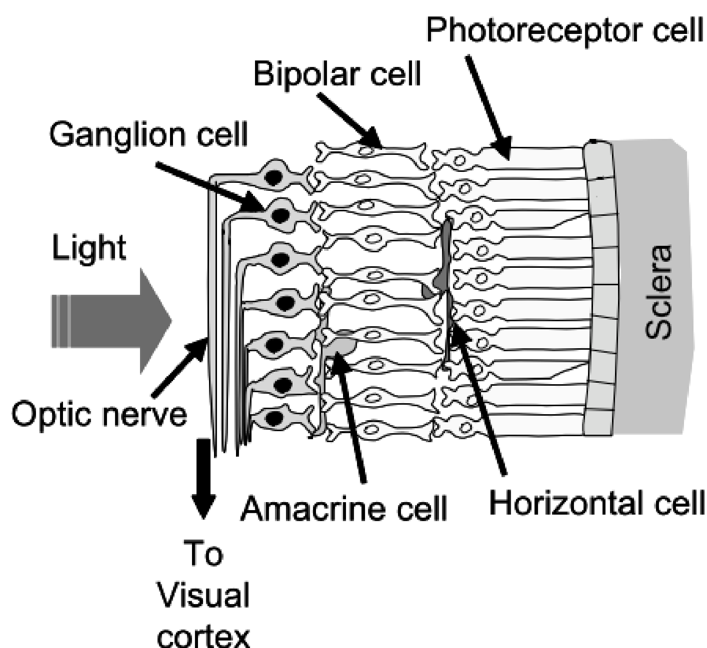


Figure 3.4: The structure of human retina [61]

In the Figure 3.5(a), an example of one-dimensional focal plane array with ten photodetectors namely $P1$ until $P10$ is shown. The photodetector cells (P) represent a focal plane array ultraviolet photodetector which receive the ultraviolet radiation from the hydrogen flame and generate photocurrents. A bright object, which represents a ultraviolet radiation, hits $P1$ to $P5$. While $P6$ until $P10$ remains dark, which means that no ultraviolet radiation hits the photodetectors. In this case, Figure 3.5(b) shows the photocurrents from the photodetectors. The horizontal cells (H) denote the resistive network which smooth the photocurrent signals from the photodetector cells (P). The output signal of the horizontal cells (H) is shown in Figure 3.5(c). The bipolar cells (B) subtract

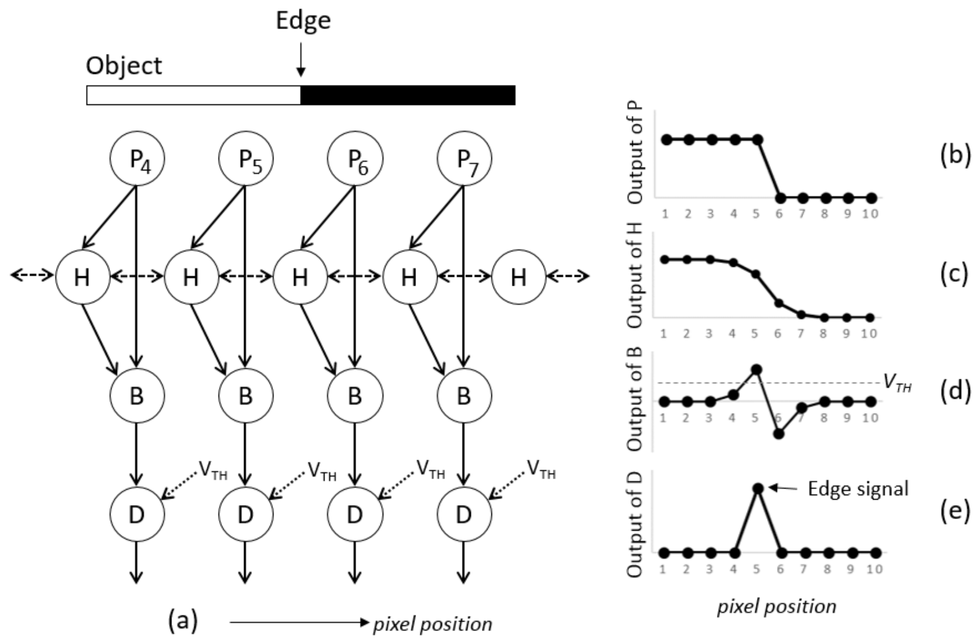


Figure 3.5: Edge detection architecture. (a) Model based on the outer vertebrate retina. (b) Output signals of photodetectors (P). (c) Output signals of horizontal cells (H). (d) Output signals of bipolar cells (B). (e) Output signals of digitized cells (D)

the signal from the photodetector cells (P) and the horizontal cells (H), the result can be seen in Figure 3.5(d). By thresholding the output signals of the bipolar cells (B), the digitized cells output the edge of the object at the photodetector number 5, as shown in Figure 3.5(e).

3.3.1 Current mirror circuit

Current mirror circuits play important role in the edge detection circuit. The current mirror circuit duplicates the current that flows in its input to its output. Basically, the photocurrent from the photodetector is copied to the horizontal cell and to the bipolar cell. At the digitized circuit, the current mirrors copy the current from the bipolar cell and from the threshold current.

The basic of current mirror circuit from NMOS transistors is shown in Figure 3.6. The schematic used 4-terminals NMOS transistor with the source is connected to the ground. The $M1$ transistor is diode-connected meaning that the gate is connected to the drain. In a diode-connected configuration, the V_{GS} is equal to the V_{DS} meaning that the transistor is always in the saturation region. In saturation region, an NMOS transistor has equations as in eq. 3.7

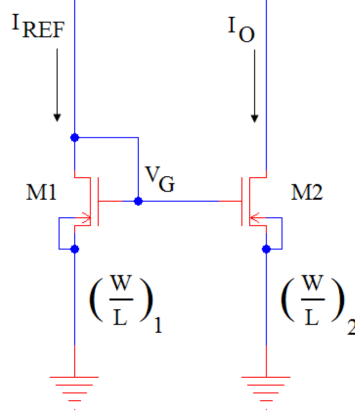


Figure 3.6: Basic current mirror from NMOS transistors

$$\begin{aligned} V_{DS} &\leqslant V_{GS} - V_{TN} \\ I_{DS} &= \frac{1}{2}\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \end{aligned} \tag{3.7}$$

where V_{DS} is the voltage of drain relative to the source, V_{GS} is the voltage of gate relative to the source, V_{TN} is the threshold voltage of NMOS transistor, I_{DS} is the current from drain to the source, μ_n is the carrier mobility, C_{OX} is the gate oxide capacitance which is equal to the dielectric constant of silicon dioxide divided by average thickness of the gate oxide, W is the gate width, L is the channel length, and λ is the channel length modulation effect. In Figure 3.6, The V_{GS} of $M2$ is equal to the V_{GS} of $M1$. In addition, when it is assumed that $M1$ and $M2$ are fabricated at the same condition result then the carrier mobility and the gate oxide capacitance have the same value.

$$I_{DS_{M1}} = I_{REF} = \frac{1}{2}\mu_n C_{OX} \frac{W_{M1}}{L_{M1}} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \tag{3.8}$$

$$I_{DS_{M2}} = I_O = \frac{1}{2}\mu_n C_{OX} \frac{W_{M2}}{L_{M2}} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \tag{3.9}$$

Substituting eq. 3.8 into eq. 3.9 results eq. 3.10.

$$I_O = I_{REF} \left(\frac{W_{M2}/L_{M2}}{W_{M1}/L_{M1}} \right) \tag{3.10}$$

From eq. 3.10, one can notice that the reference current is able to be increased or decreased by adjusting the width and/or the length of the transistors.

3.3.2 Resistive network

The horizontal cells (H) in Figure 3.5(a) smooth the generated photocurrents produced by the photodetector cells (P). The smoothing process is done by taking the average value between two adjacent nodes. Simply by adding a resistor to the two adjacent nodes can realize a resistive network. A resistor can be fabricated using diffusion, polysilicon, or well. Table 3.2 shows the device characteristic of the resistor from the C5 process family (0.5 μm) from ON Semiconductor. However, it takes a wide area to have a large resistor value. So, it is preferable to use MOS transistor as a resistor. A resistive network has been proposed in many styles. In this thesis work, the resistive network was fabricated using a single PMOS transistor (the PMOS $MP4$ in Figure 3.10). The reasons are to simplify the circuit and to use the area as small as possible.

Table 3.2: MOS resistor characteristic of C5 process family from ON Semiconductor

Resistor type	**Typical value of sheet resistivity (Ω/square)**
N-Diffusion	80
P-Diffusion	110
Poly	25
Hi-R Poly	1000
N-Well	855

A PMOS as a resistor has non-linear characteristic. But at a specific working range, we can get an almost linear characteristic. As described in Table 3.1, the generated photocurrent of 14.1 fA - 14.1 nA will give voltage drop of 1.97 - 295.67 mV on the silicon diode. This voltage range works in the sub-threshold region of the MOS transistors. When the simulation was carried out, a 1.5 μm process technology with SPICE (Computer Simulation Program with Integrated Circuit Emphasis) parameters level 3 was used. Since the SPICE parameter level 3 does not produce an accurate simulation on the sub-threshold region, an offset voltage of 1.6 V was added to the silicon diode to force the system working in the saturation or active region. From the simulation, the voltage on the $R1$ (in Figure 3.10) also on the $R2$ will be in the range of 1.609 V - 1.897 V. This means that the possible voltage difference is 288.04 mV.

Figure 3.7 shows the SPICE simulation to evaluate the resistance value of a PMOS with the gate length and width are 15 μm and 10 μm, respectively. The gate is grounded and the substrate is

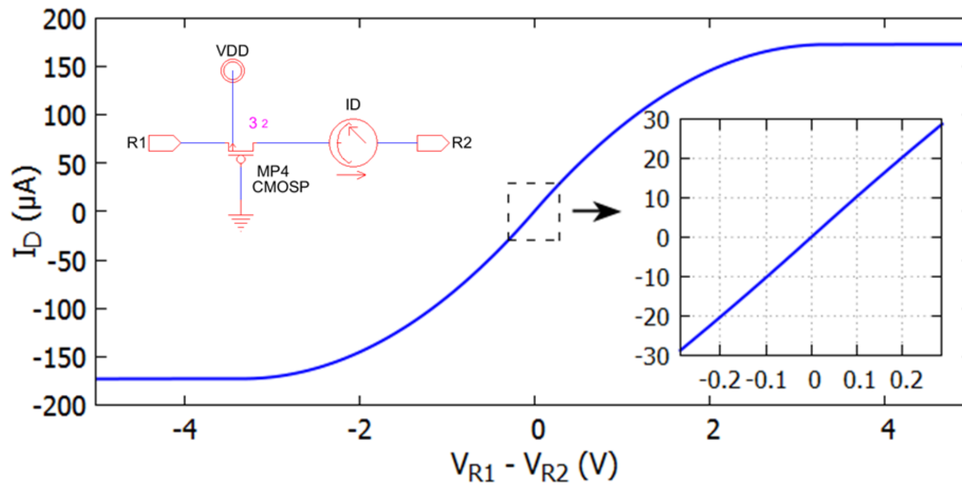
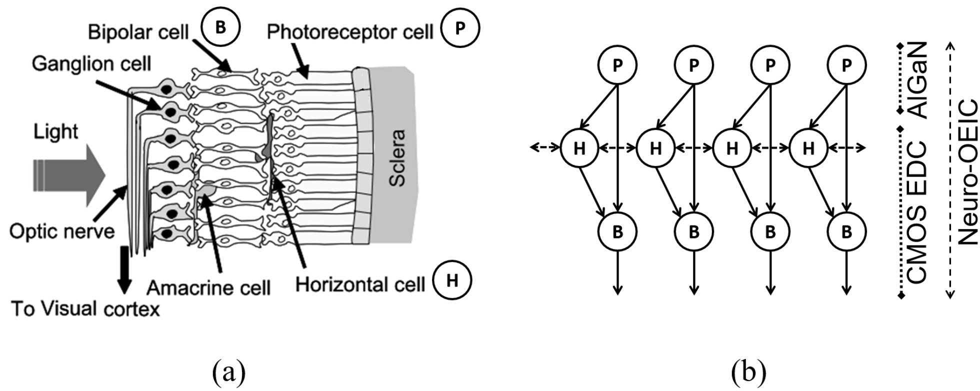


Figure 3.7: Using a PMOS as a resistor at a specific working range. The left inset shows the schematic for simulation and the right inset shows the specific working range of the PMOS at the dotted rectangle region

connected to the positive power supply. The supply is 5 V. The schematic of the simulation circuit is shown in the inset picture at the left side. The source and drain terminals, $R1$ and $R2$, are swapped from -1 V to 1 V to see the responses. Then, the inset picture at the right side shows the working range of the PMOS in the edge detection circuit. An almost linear current response can be obtained in this working range (-288.04 mV to 288.04 mV) and the average resistance value, which is the slope at the working range, is 10,013 Ω or about 10 kΩ.

3.3.3 Neuro-OEIC device structure

The outer human (vertebrate) retina model will be implemented as a neuro-OEIC device. The photoreceptor cells were implemented as a sapphire-based BSI-SBD UV focal plane array while the horizontal cells and bipolar cells are implemented as a silicon-based edge detection circuit. Figure 3.8 shows the illustration of the partition of the implementation. The focal plane array and edge detection circuit are fabricated separately. Then, the focal plane array will be stacked onto the edge detection circuit using microbumps as shown in Figure 3.9.



(a) (b)

Figure 3.8: Neuro-OEIC device structure. (a) Human retina structure. (b) Retina model as neuro-OEIC

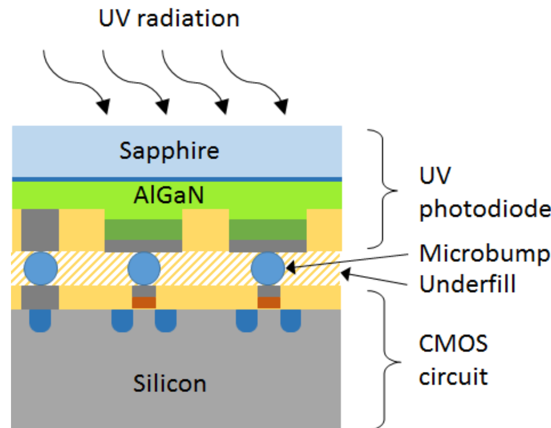


Figure 3.9: Proposed neuro-OEIC device structure

3.4 Circuit schematic design

The schematic of the edge detection circuit was drawn using Electric 9.05. Figure 3.10 shows the schematic of the edge detection circuit.

In Figure 3.10, the photocurrent I_P from photodiode is inputed to the cathode of the silicon diode $D1$. The voltage drop of the silicon diode $D1$ is used to drive the NMOS MN1 to generate current I_{P*}. Two current mirrors copy the I_{P*}. The first is the PMOS MP1 and MP2 that copy the I_{P*} as the I_H that acts as the input to the horizontal cell circuit. The second is the PMOS MP1 and MP3 that copy the I_{P*} that acts as the input to the bipolar cell circuit. The PMOS MP4 works as the resistive network. When the source and drain terminals of the PMOS MN4 have a voltage different, current I_R will flow and change the value of the current I_H. If there is no voltage different at PMOS

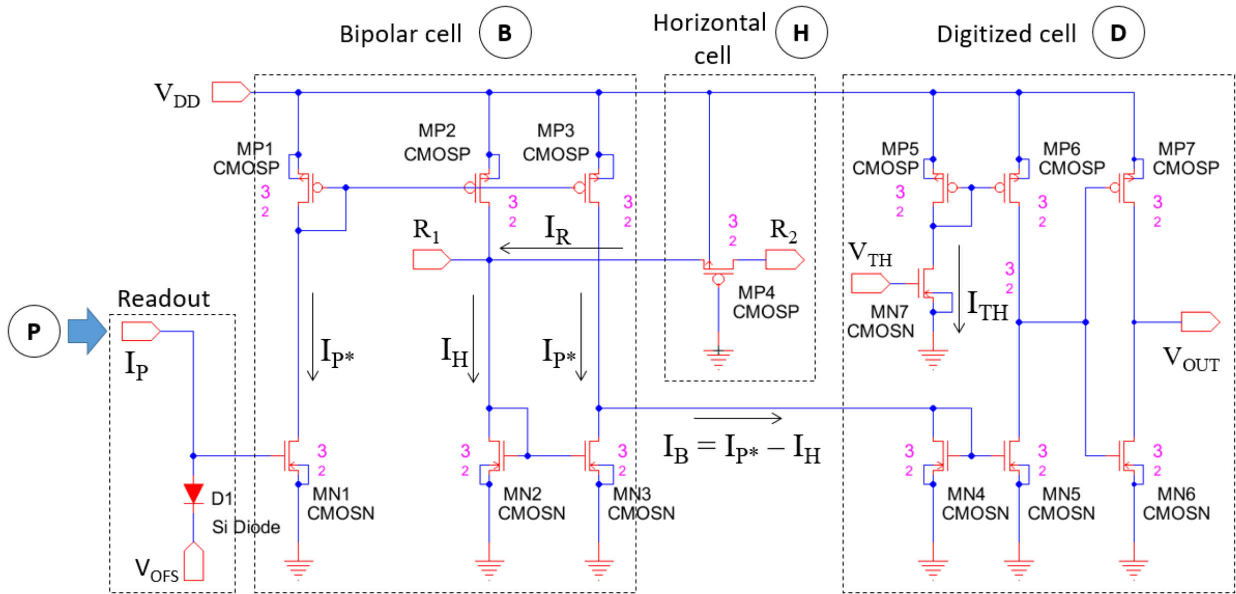


Figure 3.10: Schematic of edge detection circuit

MN4's terminals, then the value of current I_H does not change. Next, the NMOS MN2 and MN3 copy the current I_H. The PMOS MP3 and the NMOS MN3 serve as the bipolar cell circuit that subtracts the copied photocurrent I_{P*} and copied current I_H to produce a current I_B. The current I_B from the bipolar cell circuit is then duplicated by a current mirror NMOS MN4 and MN5, to be compared with the threshold current I_{TH} that comes from the current of MNOS MN6 and is mirrored by PMOS MP5 and MP6. Finally, to have a sharp edge response, an inverting circuit of PMOS MP7 and NMOS MN7 is added.

3.5 Circuit simulation

The edge detection circuit was simulated using LTspice IV. In simulating the circuit, a 1.5 micron process technology with SPICE parameter level 3 was used. As explained previously, the SPICE parameter level 3 can not simulate the sub-threshold region. In this case, an offset voltage of 1.6V was added for a VDD of 3.0 V, so that the transistors work in the active region only. The circuit was simulated in one-dimensional array and two-dimensional array which their connections are shown in Figure 3.11 and Figure 3.12, respectively.

In Figure 3.11, a connection of one-dimensional array of 6 pixels is shown. Figure 3.11(a) is a unit pixel for one-dimensional array which is a representation of Figure 3.10 with the PMOS MP4 as the resistive network is drawn as a blue-filled small rectangle, while the rest of the components are

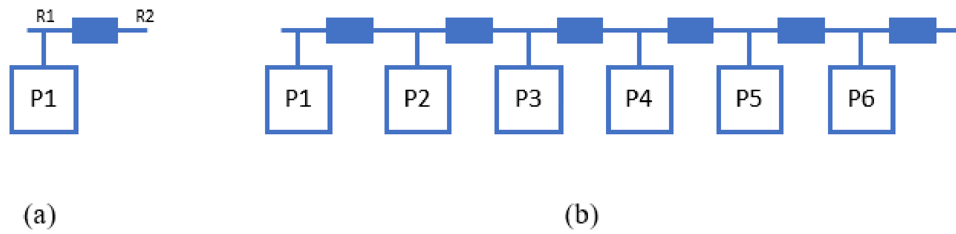


Figure 3.11: One-dimensional array connection. (a) A unit pixel for one dimensional array. (b) An example of one-dimensional array of 6 pixels

illustrated as a white rectangle with the index P-*n* meaning a pixel number-*n*. In a one-dimensional array connection of six pixels, Figure 3.11(b) shows this example. The resistive network connects the two adjacent pixel. For the most right side, the resistive network is left unconnected.

For two-dimensional array, the connection is shown in Figure 3.12. A unit pixel for two-dimensional array is shown in Figure 3.12(a). Since there will be horizontal and vertical pixels connection, there are two resistive networks for horizontal connection and vertical connection, respectively. Figure 3.12(b) shows an example of a two-dimensional array of 6 x 4 pixels. The most right side and the most upper side of the resistive networks are left unconnected.

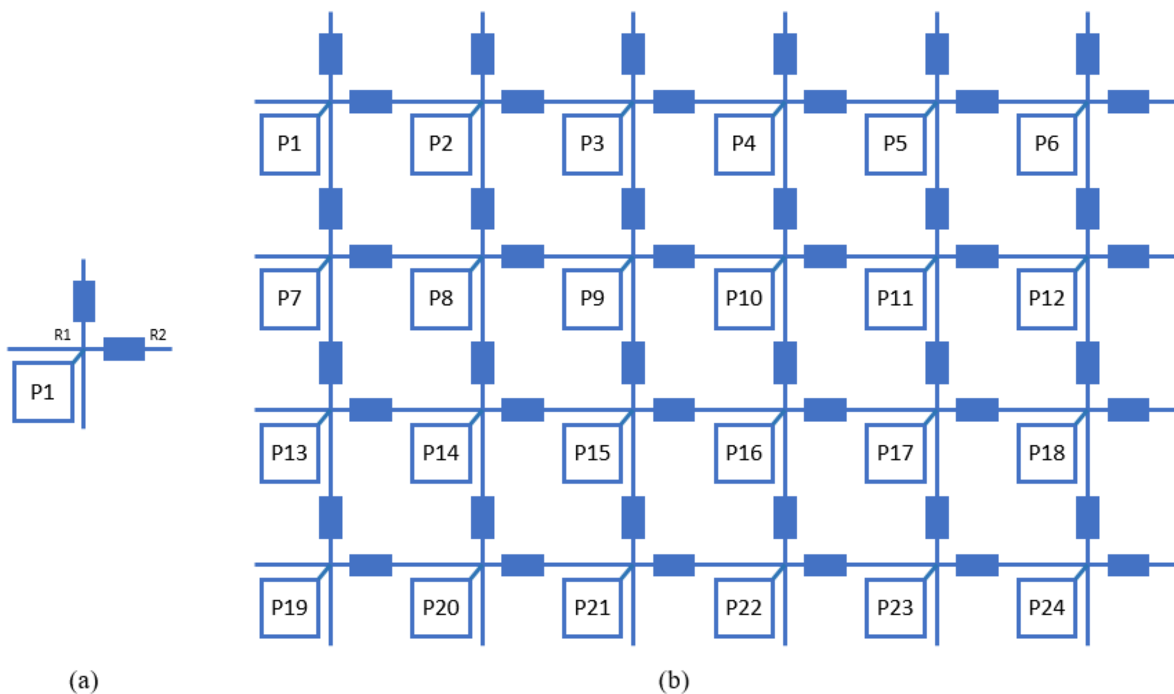


Figure 3.12: Two-dimensional array connection. (a) A unit pixel for two-dimensional array. (b) An example of two-dimensional array of 6 x 4 pixels

3.5.1 One-dimensional simulation

The simulation result of a one-dimensional array with 1 x 80 pixels is shown by Figure 3.13. The VDD, the V_{OFS}, and the V_{TH} were 3.0 V, 1.6 V, and 1.64 V respectively. The threshold voltage of the PMOS and NMOS are -1.6 V and 1.6 V, respectively. The width and length of all transistor are 15 μm and 10 μm, respectively. The x-axis of Figure 3.13 represents the pixel numbers. In Figure 3.13(top), the input current was simulated as a step stairs pattern to indicate the edges with the increment of a decade at every 10 pixels, started from 0.1 pA until 1 μA. Figure 3.13(middle) shows that when the input current changed, meaning that the values between two adjacent pixels are different, the bipolar cells produced spike. In this case, it can be concluded that the circuit was able to detect the edges. A threshold current of 109.6 nA was chosen and compared with the spikes. When the spike is above the threshold current then the digitized circuit generates a pulse which is labeled as a binary "1", as shown in Figure 3.13(bottom).

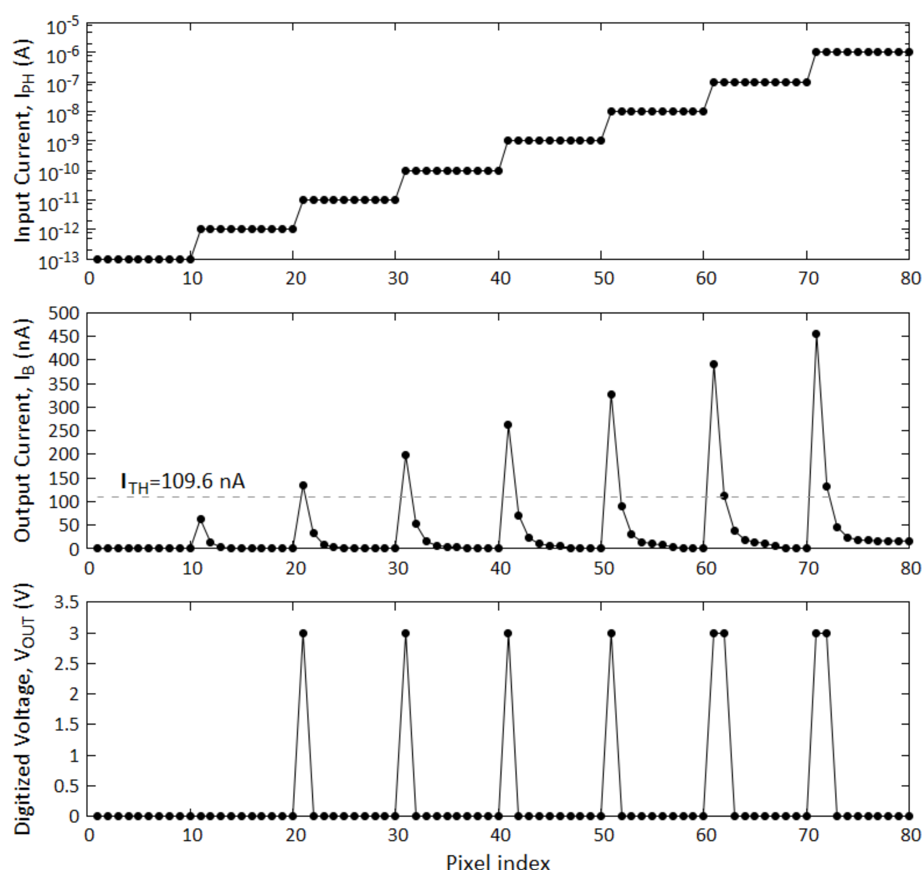


Figure 3.13: One-dimensional array of 1 x 80 pixels' simulation result. (top) Input current generated from photodiode. (middle) Output current of the bipolar cells with a threshold current. (bottom) Output voltage of the digitized circuits

As described previously, the bipolar cell subtracts the current from the photodiode and the horizontal cell, which is shown in Figure 3.14. Figure 3.14 only focuses on the pixel number 26 until pixel number 37. In Figure 3.14(top), the current I_{P*} (in Figure 3.10) was marked with the filled circles while the current I_H from the horizontal cell was marked with the stars. It is shown that the horizontal cells smooth the current I_{P*}. As a result, by subtracting both currents produces a signal as shown in Figure 3.14(middle). Since in the designed circuit there is no negative supply, the result of the subtracting process is only positive signal, as shown in Figure 3.14(bottom). It can be seen that when the edge occurred at the pixel number 30 and 31, a spike was generated at the pixel number 31. So, the edge position can be detected by observing the spike at the output of the bipolar cells.

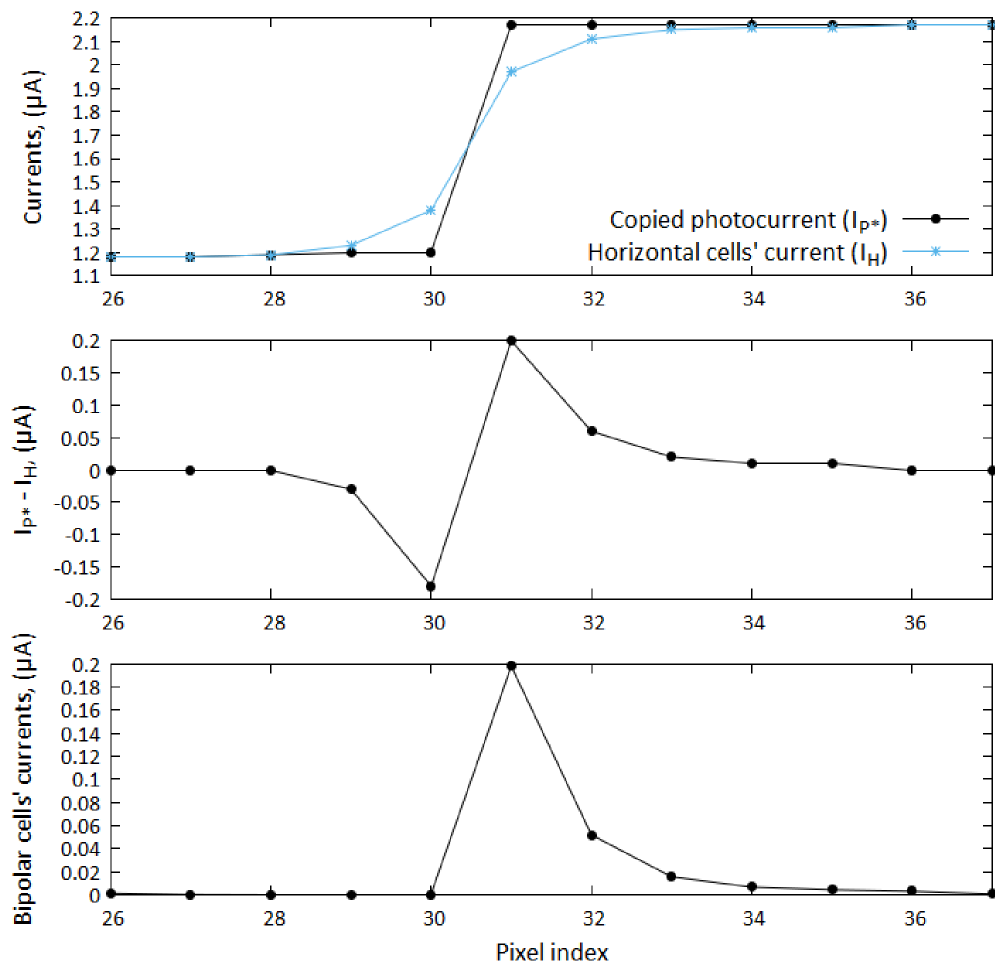


Figure 3.14: Subtraction process. (top) A step pattern in photocurrents and the smoothed pattern produced by the horizontal cells. (middle) The subtraction between the step pattern and the smoothed pattern mathematically. (bottom) The output current of bipolar cells in the edge detection circuit

3.5.2 The effect of resistive network values

Some researchers use linear resistor or local adaptation resistor to provide the resistive network. [62] [63] [64] However, because of the area consumption issue, we chose a PMOS as the resistor which has a non-linear resistivity characteristic. We simulated the effect of the resistor value around the out PMOS-resistor value. In our design, the PMOS as the resistor has an average resistivity of 10 kΩ in a working voltage range of ±288.04 mV. When the PMOS is compared with fixed resistors with the same given photocurrent as Figure 3.13(top), the current outputs of the bipolar cells are shown in Figure 3.15

To have a clear image, the peaks of each spike in Figure 3.15 are connected as a line. The peaks were determined at the pixel number 11, 21, 31, 41, 51, 61, and 71. The result is shown in Figure 3.16. Using a PMOS as the resistive network has a similar characteristic with fixed resistors with the resistivity value less than 100 kΩ. Resistivity values from 12 kΩ to 100 kΩ result the peak of the spike becomes higher with the increase of the photodiode current. Meanwhile, a fixed resistor of 1 MegΩ has an almost flat peaks. In a flat peaks, it is easy to have a universal threshold voltage that works for every peaks. While in an increasing peaks, a small changes in the photodiode current can be ignored by raising the threshold voltage.

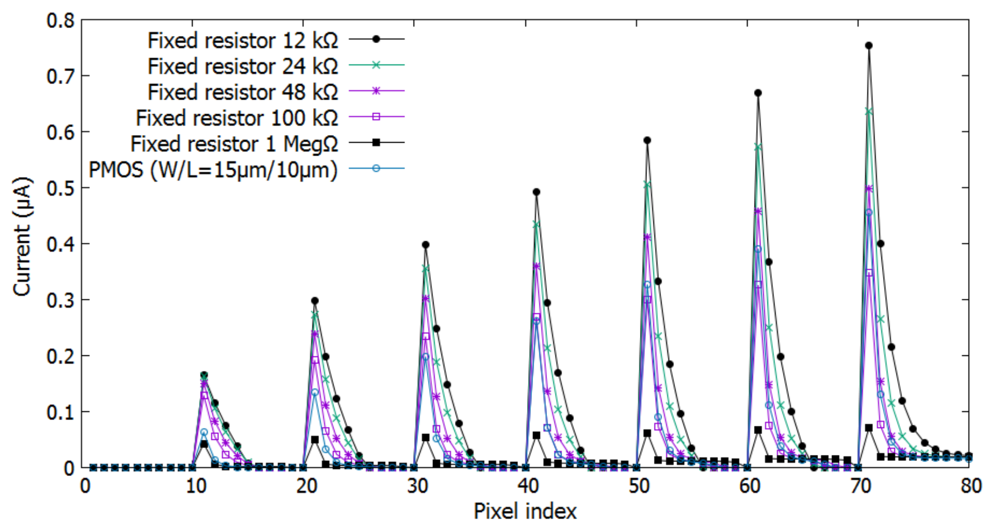


Figure 3.15: The output current of bipolar cells with different resistor values

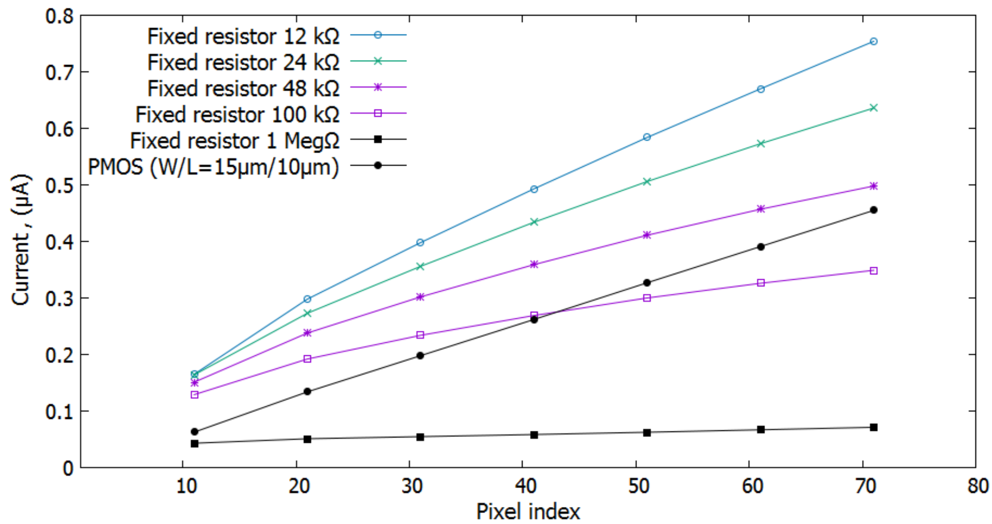


Figure 3.16: The trend of the peak of the bipolar cells' output

3.5.3 Two-dimensional simulation

For two-dimensional array simulation, 45 × 45 pixels was connected with configuration as shown in Figure 3.12(b). Two-dimensional array simulation may take time depending on the performance of the personal computer that is used. Also, drawing the schematic for two-dimensional array is not an easy task. In this case, a program written in Processing software was used to create a large SPICE code. Then, the SPICE code was simulated using Cadence in our servers instead of using LTspice. The VDD, the V_{OFS}, and the V_{TH} were 3.0 V, 1.6 V, and 1.64 V, respectively. The threshold voltage of the PMOS and NMOS were -1.6 V and 1.6 V, respectively. The width and length of all transistors were 15 μm and 10 μm, respectively. Figure 3.17 shows the simulation results. The y-axis on the left side and the x-axis represent the pixel numbers from 0 to 44, while the y-axis on the right side show the image color that represents the current values or the voltage values.

The input was given as an image that has a burning flame shape, as shown in Figure 3.17(a). Each pixel value within the image in Figure 3.17(a) was normalized from 0 to 1 nA to simulate the photocurrents. The outputs current of the bipolar cells were normalized from black to white as shown in Figure 3.17(b). By applying a threshold voltage of 1.64 V in the digitized circuit that produces a current of 109.6 nA, the result was binary voltage outputs of 0 V and 3 V as shown in Figure 3.17(c). When the range of the simulated photocurrents were increased from 0 to 100 nA as shown in Figure 3.17(d), the output current of the bipolar cells were more thicker as shown in Figure 3.17(e) comparing to Figure 3.17(b). The binary image result from the digitized circuit was

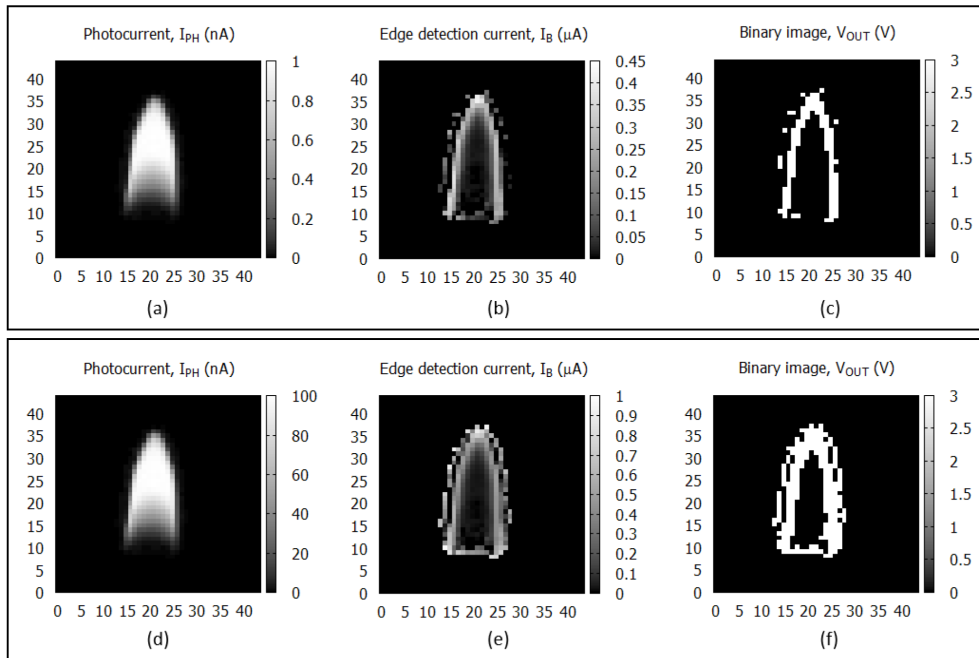


Figure 3.17: Two-dimensional array of 45 x 45 pixels' simulation result. (a) Input current from 0 to 1 nA. (b) Edge detection current with the input current from 0 to 1 nA. (c) Binary image with the input current from 0 to 1 nA. (d) Input current from 0 to 100 nA. (e) Edge detection current with the input current from 0 to 100 nA. (f) Binary image with the input current from 0 to 100 nA

also became more thicker as shown in Figure 3.17(f) comparing to Figure 3.17(c).

The simulation results show that the edge detection circuit and the digitized circuit were worked successfully. However, the more higher the current input the more thicker the edges. This phenomena can be explained using Figure 3.13. With an increasing peaks pattern as shown in Figure 3.13(b), choosing the global threshold is an important decision. In Figure 3.13(b), for the last two spikes, there are two pixels above the threshold. As the result, in Figure 3.13(c), the last two spikes have two points of logic-1 instead of one point. This means that the binary image resulted thicker detected edge. In this case, if the thickness of the detected edge is important then to have a flat peaks characteristic of the current output of the bipolar cells should be considered.

3.6 Circuit layout design

In this section, the design rules is briefly introduced. Then, the edge detection circuit layout is described.

3.6.1 Design rules

When designing the circuit layout, a design rules must be obeyed. Transistor channel length is the distance between source and drain of a transistor and is set by the minimum width of a polysilicon wire. The minimum channel length is called as feature. The main objective of design rules is how to make a fine pattern and how to make a high packing density in a particular fabrication process. Design rules is also related to design ability such as the lithography ability, etching ability, etc. Design rules does not define the electrical characteristics. In general, design rules represent a compromise between performance and yield. When the design rules is more conservative (traditional or simple), it is more likely that the circuit will work. However, when the design rules is more complex or aggressive, it will improve the performance and size of the circuit.

Usually, industrial specifies design rules in microns and each of them might have different design rules. To make the migration of the layout design to a different foundry's process easier, Mead and Conway popularized a scalable design rules based on a single parameter, λ, that characterizes the resolution of the process. λ is generally half of the minimum drawn transistor channel length. This is called as Lambda (λ) Rules. The derivation of some λ rules based on a representative set of micron rules is shown in Table 3.3.

Table 3.3: Derivation of lambda-based rules from micron rules

MASK	FEATURE	DIMENSIONS	
		Micron rule	λ rule
1: Thinox	Minimum thinox width	4 μm	2λ
	Minimum thinox spacing	4 μm	2λ
	Minimum p-thinox to n-thinox spacing	8 μm	4λ
3: Polysilicon	Minimum poly width	3.75 μm	2λ
	Minimum poly spacing	3.75 μm	2λ
	Minimum gate poly width (p)	4.5 μm	3λ
	Minimum gate poly width (n)	4.0 μm	2λ
	Minimum gate poly extension	3.5 μm	2λ
6: Aluminum	Minimum Al width	4.5 μm	3λ
	Minimum Al spacing	4.5 μm	3λ

For example, a 1 μm process has a minimum polysilicon width (and hence transistor length) of 1 μm and uses design rules with λ of 0.5 μm. Lambda-based rules are necessarily conservative because they round up dimensions to an integer multiple of λ. However, they make scaling layout trivial; the same layout can be moved to a new process simply by specifying a new value of λ. Below 180 nm, design rules have become so complex and process specific that scalable design rules are difficult to apply.

Figure 3.18 shows the simplify lambda-based design rules from MOSIS. The MOSIS service *(http://www.mosis.com)* is a low-cost prototyping service that collects designs from academic, commercial, and government customers and aggregates them onto one mask set to share overhead costs and generate production volumes sufficient to interest fabrication companies. It is called as Multi Project Wafer services. MOSIS has developed a set of scalable lambda-based design rules that covers a wide range of manufacturing processes. The rules describe the minimum width to avoid breaks in a line, minimum spacing to avoid shorts between lines, and minimum overlap to ensure that two layers completely overlap.

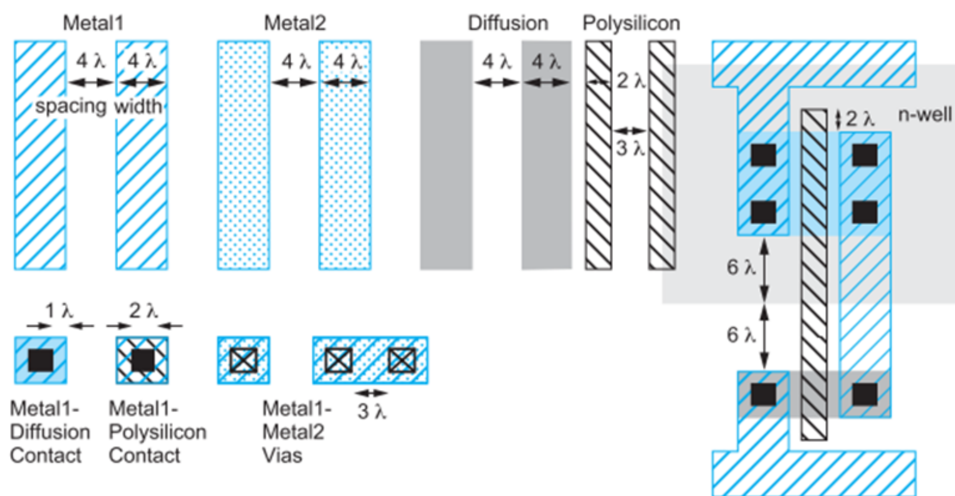


Figure 3.18: Simplify lambda-based design rules [65]

3.6.2 Edge detection circuit layout design

The edge detection circuit layout was drawn using Electric VLSI software in 5 micron lambda-design rules with one polysilicon layer and one metal layer. This means the feature size is 10 μm. The area size of the edge detection circuit layout is about 1 mm x 0.7 mm. The layout for a single pixel of the edge detection circuit is shown in Figure 3.19. The dashed-polygons show each function of the circuit. They are the readout circuit, bipolar cell circuit, horizontal cell circuit, and digitized cell circuit. The readout circuit consists of a silicon diode and a NMOS. The bipolar cell circuit consists of 3 PMOS and 2 NMOS transistors. The horizontal cell circuit uses a PMOS. The digitized cell circuit consists of 3 PMOS and 4 NMOS transistors. The PMOS transistors were placed at the top side while the NMOS transistors were located at the bottom side. The polysilicon layer inside the circuit had a width of 10 μm. The polysilicon layer was used as a connector when

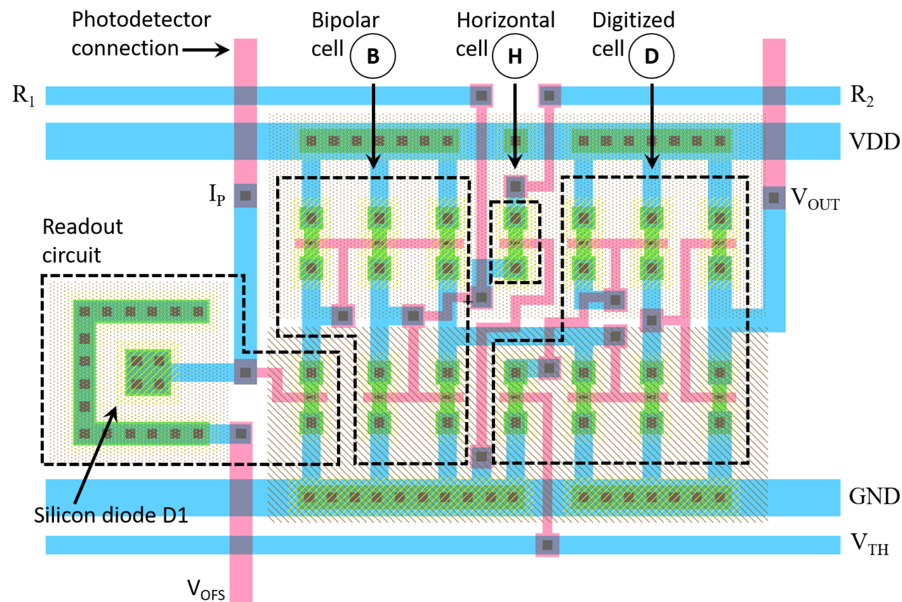


Figure 3.19: A layout of one pixel of the edge detection circuit

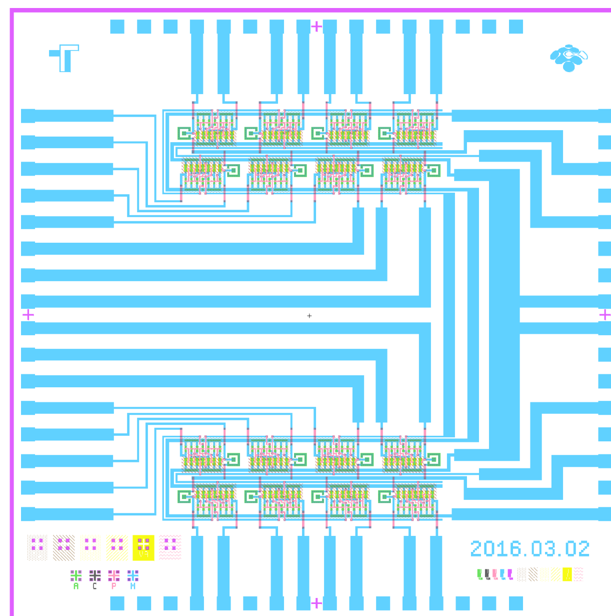


Figure 3.20: A layout of the edge detection circuit of 1 x 16 pixels

the path crosses the metal layer, since only one metal layer was selected for the fabrication process.

In this thesis, a one-dimensional array of 1 x 16 pixels was fabricated to demonstrate the concept. Appendix C shows the simple calculation for estimating the required number of pixel that should be fabricated. The arrangement of the circuit is shown in Figure 3.20. It was intended that

the chip will be bonded to a 64-pins package.

3.7 Circuit fabrication

The edge detection circuit was fabricated by using the facilities of the Venture Business Laboratory (VBL) and Electronics-Inspired Interdisciplinary Research Institute (EIIRIS) in Toyohashi University of Technology. The process technology of 1.5 micron was used. Some typical process characteristics is shown in Table 3.4.

Table 3.4: Process characteristics

Operating voltage	5, 12 V
Substrate material	P-type, bulk or EPI
Drawn transistor length	1.5 μm
Gate oxide thickness	30 nm
Field oxide thickness	800 nm
Polysilicon thickness	300 nm
Metal thickness	1 μm
Metal composition	AlSi

The substrate material was made by Czochralski process, a p-type (Boron doped) 2-inch wafer with <100> orientation, the thickness was 280.0 $\pm$ 25.0 μm, and the resistivity was 1.49 $\sim$ 1.63 Ω. To calculate the initial doping concentration of the substrate material, Figure 3.21 is used, and the substrate material has Boron concentration of about 1 x 10^{16} cm^{-3}.

The process steps were modified comparing to the standard CMOS process. In this case, the LOCOS step was omitted to shorten the fabrication time. In this process, since the Boron dopant has a low concentration near the surface, a channel stopper process for NMOS transistors was added. The process steps are shown in Table 3.5 while the fabricated chips is shown in Figure 3.22. The fabricated EDC chip had an area of 875 x 600 μm^2.

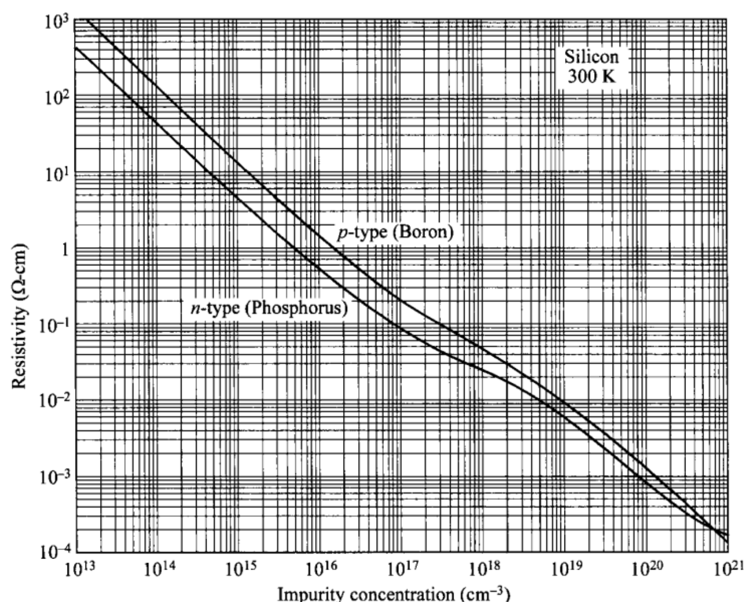


Figure 3.21: Impurity concentration versus resistivity of the silicon substrate

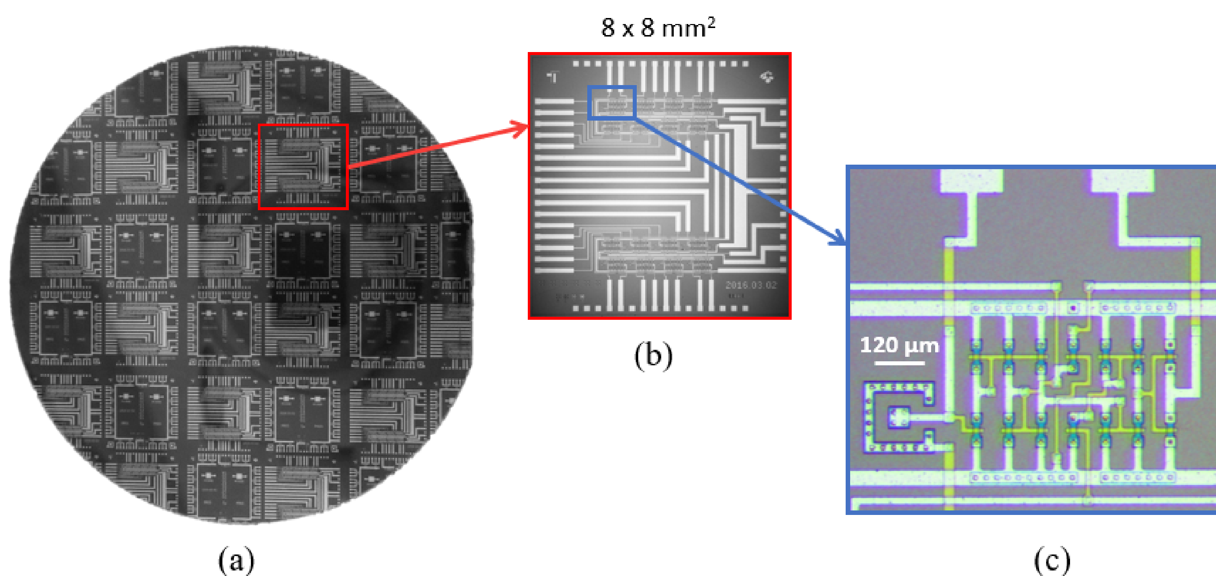


Figure 3.22: Photograph of the fabricated chips. (a) The 2 inch wafer contains several edge detector circuit chips and test element group chips. (b) The edge detector circuit chip. (c) A pixel circuit

3.8 Experimental result and discussion

After the fabrication finished, a wafer level testing was conducted. The equipment setup is shown in Figure 3.23. There were a personal computer, Agilent 4155C Semiconductor Parameter Analyzer, Agilent 16442A Test Fixture, and 64-pins probe cards inside a probe station. The Easy

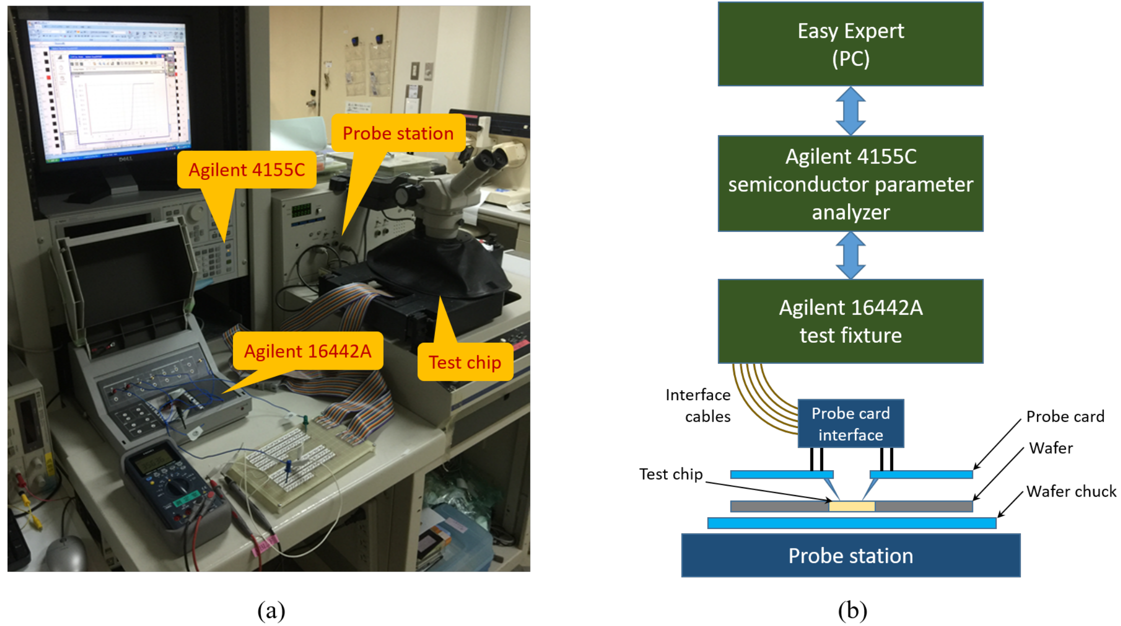
Table 3.5: Process steps

Process	**Remark**
Alignment mark formation	Used for aligning pattern in photolithography
P-well formation	Boron implantation
N-well formation	Phosphorus implantation
Drive-in annealing	Recovering crystal damage after implantation
Channel stopper for NMOS	Increasing threshold voltage for non NMOS area
Active area formation	Field oxide formation and opening area for MOS, diode, and contact
Threshold voltage adjust	Adjusting NMOS threshold voltage
Gate formation	Gate oxide and N-type polysilicon formation
Source/drain N-diffusion	NMOS source/drain diffusion
Source/drain P-diffusion	PMOS source/drain diffusion
Activation annealing	Recovering crystal damage after implantation
Contact formation	Preparing holes for metal contact
Metalization	Sputtering and patterning the metal wires
Sintering	Lowering contact resistivity

Expert software controls the Agilent 4155C and displays the measured data in the monitor as graphs or makes log-files. The Agilent 16442A is the test fixture for the Agilent 4155C. The Agilent 16442A has input/output channels that connect to the fabricated chip through the interface cables.

The silicon diode was measured to get the I-V curve which is shown in Figure 3.24. During the measurement, the diode's voltage was swept from -5.0 V to 5.0 V. From the I-V curve of the measured silicon diode, the characteristic of the silicon diode is shown in Table 3.6.

The MOS transistors in the test element group chips was evaluated because it is difficult to evaluate an individual MOS transistor inside the circuit. The MOS transistors was measured to get



(a) (b)

Figure 3.23: Equipment setup. (a) The equipments. *Photograph*: Clean Room, Toyohashi University of Technology. (b) Diagram of the equipment setup

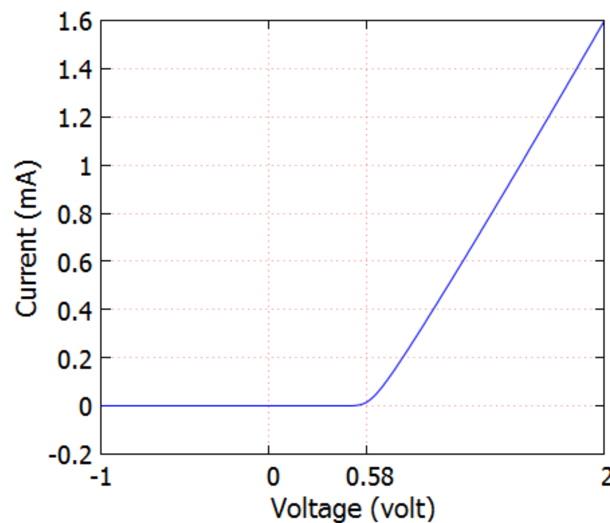


Figure 3.24: The I-V curve of the silicon diode

the I_D-V_{DS} curve and the I_D-V_{GS} curve which are shown in Figure 3.25 and Figure 3.26, respectively. From those data, the characteristic of the MOS transistor is summed up as shown in Table 3.7. After confirming the silicon diode and MOS transistors characteristic, the next step is to confirm the edge detection circuit. The suitable value of V_{TH} (threshold voltage) to digitize the image should be determined.

Table 3.6: Silicon diode characteristics

Forward voltage V_F	0.58 V
Leakage current	-0.64 nA (at V_D = -1.0V)
	-6.7 nA (at V_D = -5.0V)

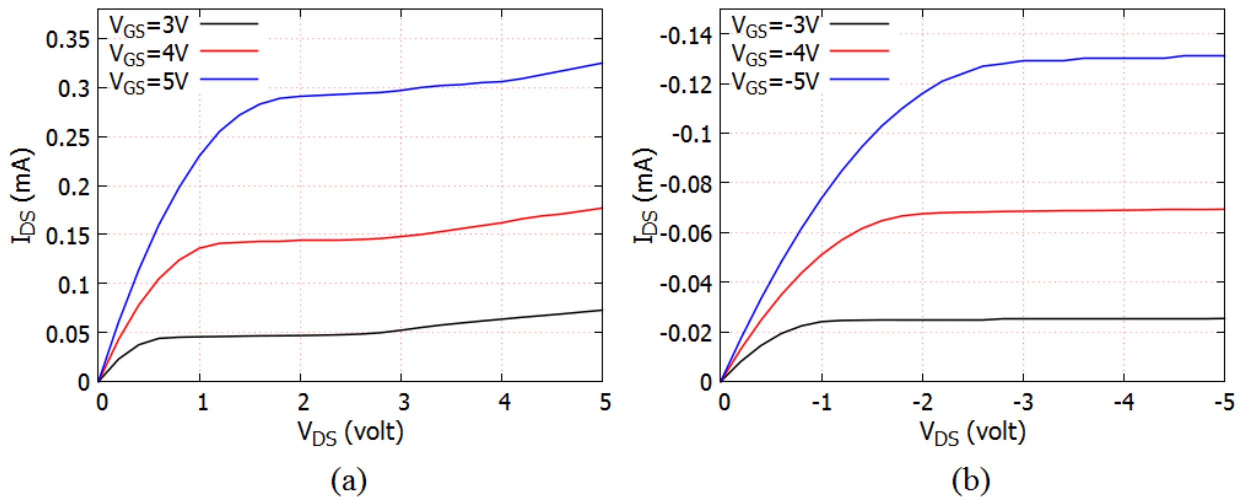


Figure 3.25: The I_D-V_{DS} curve of the MOS transistor with W/L = 15 μm/10 μm. (a) NMOS. (b) PMOS

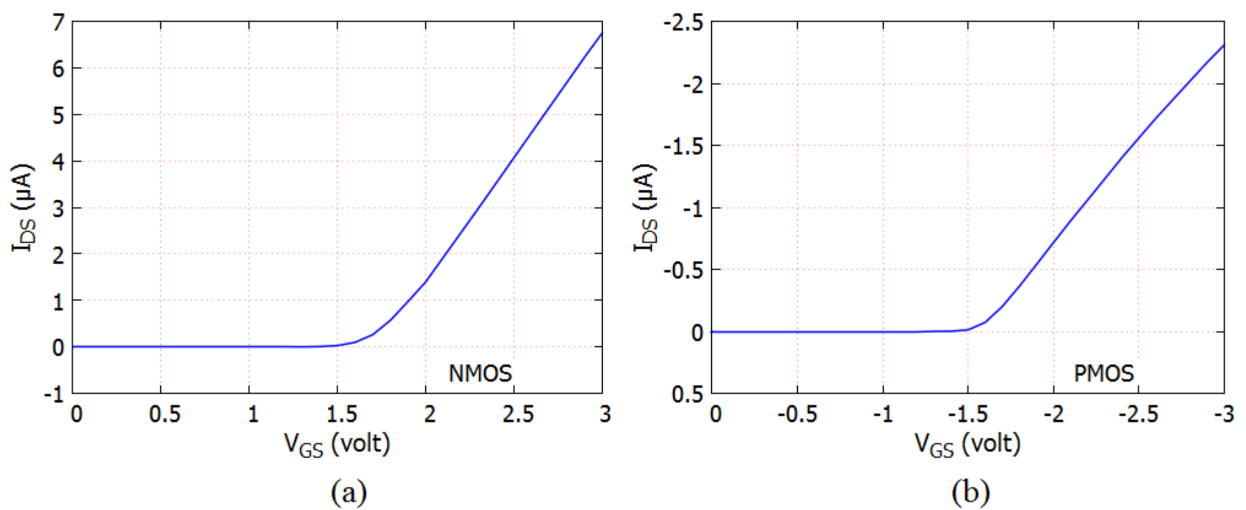


Figure 3.26: The I_D-V_{GS} curve of the MOS transistor with W/L = 15 μm/10 μm. (a) NMOS. (b) PMOS

Table 3.7: MOS transistor characteristics

NMOS	
NMOS threshold voltage V_{TN}	1.6 V
Saturation current I_{Dsat} (at V_{GS}=5V, V_{DS}=3V)	0.3 mA
PMOS	
PMOS threshold voltage V_{TP}	-1.6 V
Saturation current I_{Dsat} (at V_{GS}=5V, V_{DS}=3V)	-0.13 mA

As described in Figure 3.13, The V_{TH} produces I_{TH} that is compared to the I_B for generating binary images. This was done by applying input current to the fabricated EDC chip, then the V_{TH} was varied, until an edge-pattern was observed at the outputs of the fabricated EDC chip which were connected to the LEDs. This procedures were repeated for different input current. Figure 3.27 illustrates the procedure for selecting the threshold to digitize the image. The three channels of the Agilent 16442A test fixture supplied identical currents to the inputs of the EDC chip number 5, 6, and 7, while the other channel supplied V_{TH} to the EDC chip. The V_{DD} was set to 5 V and the offset voltage V_{OFS} was set to 2.2 V. The outputs of the EDC chip number 5, 6, and 7 were

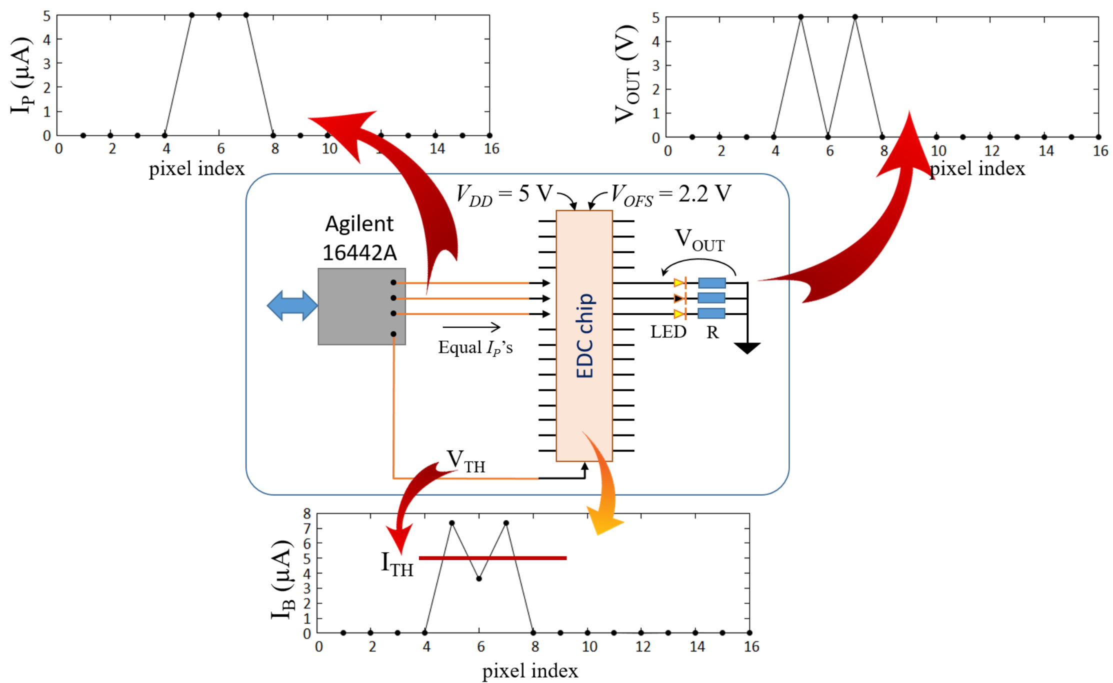


Figure 3.27: Selecting an appropriate threshold for digitizing the image

connected to the LEDs in series with 220 Ω resistor. For a given current input, the V_{TH} was varied from 2.02 V to 2.3 V, until the LEDs show a "101"-pattern, meaning that a proper threshold for generating the edges has been achieved. The process was repeated for current input in a range of 50 nA - 100 μA. The measurement result of the threshold selection for digitizing the image is shown in Figure 3.28. The dot shows where the edges was observed at the output of the EDC chip for a given threshold voltage. From this data, by choosing a threshold value of 2.2 V, the EDC chip will work for a photocurrent in a range of 100 nA - 50 μA.

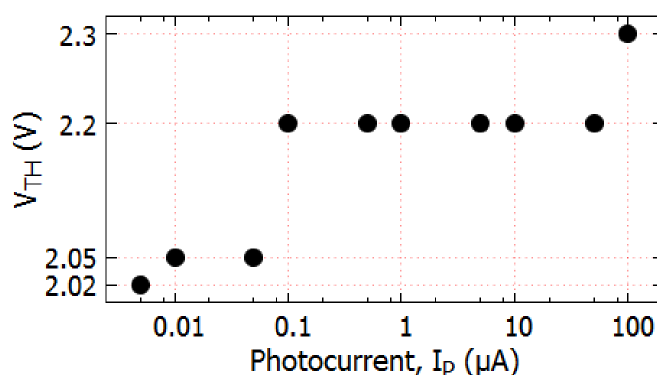
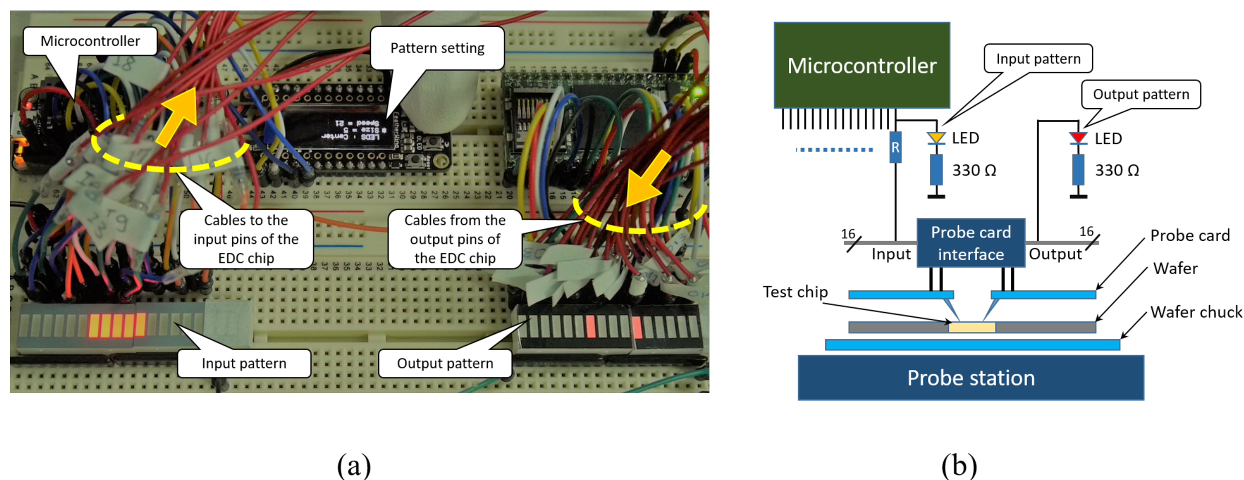


Figure 3.28: Threshold voltage selection for digitizing the image

The next is to check the response of all pixels in the fabricated EDC chip. Since the Agilent 16442A only has 3 channels to generate a constant current, a microcontroller was used to generate patterns. The output pins of the microcontroller were connected to input pins of the EDC chip in series with 100 kΩ resistors. The microcontroller's output pins generate 3.3 V for logic-1. The forward voltage of the silicon diode is 0.58 V. The V_{DD} and the V_{OFS} were set to 5.0 V and 2.2 V, respectively. With a series resistor of 100 kΩ, it was expected that a current of 5.2 μA will flow as the photocurrent which is in the range of the selected V_{TH} as shown in Figure 3.28.

The test setup is shown in Figure 3.29. The LEDs were used to give a direct visual observation on the input and output sides of the fabricated EDC chip. The generated pattern was not moving, but only the size of the pattern was modified manually by giving the microcontroller commands through the pattern setting. Figure 3.30 shows the result of the generated edge pattern. The LEDs on the left side is the input pattern produced by the microcontroller while the LEDs on the right side is the edge pattern generated by the EDC chip. From these results, it can be concluded that the fabricated EDC chip was able to detect the edge of the given object.



(a) (b)

Figure 3.29: Testing the edge pattern. (a) Circuit tester on breadboard. (b) Diagram of the equipment setup

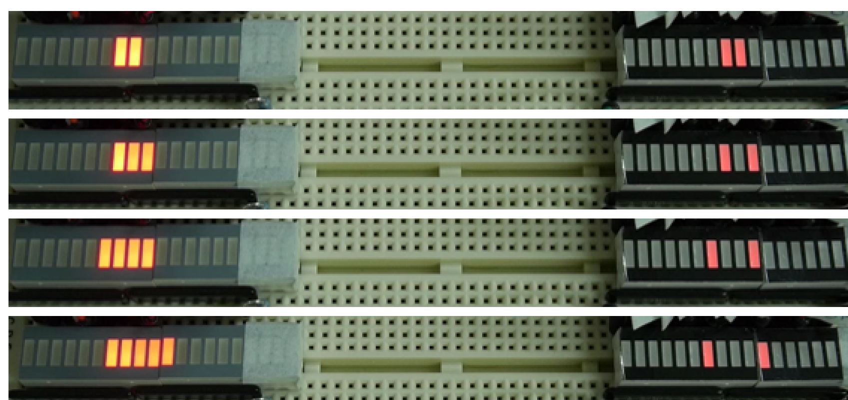


Figure 3.30: Generated edge pattern by the EDC chip (the LEDs on the right side)

There is a problem when the pattern was generated on the border of the pixels (the border means the most left side or the most right side of the pixels). The EDC did not generate edge on the pixel at the border. Figure 3.31 shows a sequence when the pattern with a size of 4 pixels was entering the detection area. When a pixel started to enter, an edge was generated. Then, when the pattern entered the detection area, no edge was generated at the pixel's border. This was continued happening until the pattern of 4 pixels completely entered the detection area by leaving the border. The same situation applied when the pattern was leaving the detection area by moving to the right side, as shown in Figure 3.32. This problem is confirmed by the simulation result of the one-dimensional array as shown in Figure 3.13. This is because the most left side pixel and the most right side pixel had unconnected resistive network.

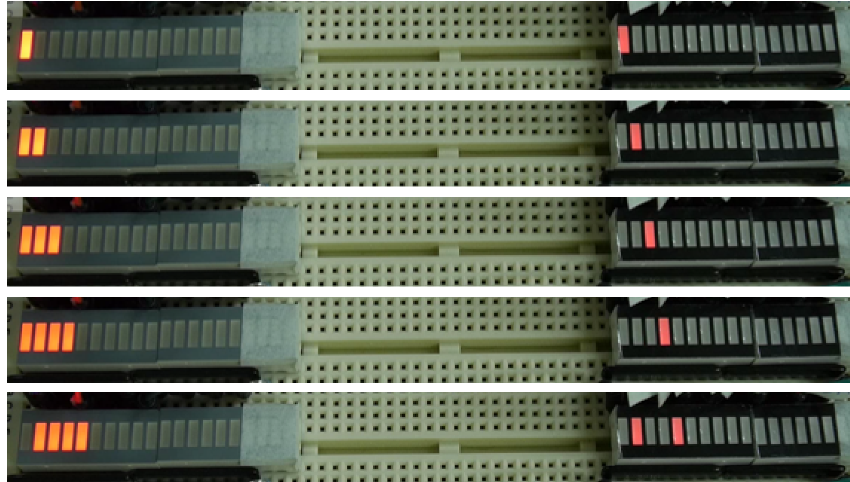


Figure 3.31: Undetected edge at the left side of border

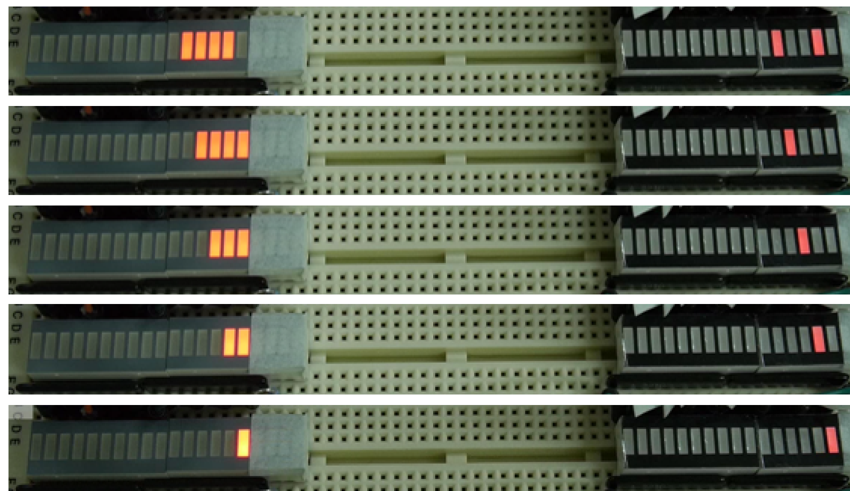


Figure 3.32: Undetected edge at the right side of border

3.9 Conclusion

The neuro-OEIC was designed to realize the biological mechanism of the outer vertebrate retina by stacking the AlGaN on sapphire BSI-SBD UV focal plane array onto the CMOS-based edge detection circuit. The outer vertebrate retina has a function as edge detection that is a very useful tools for analyzing a flame. The edge detection function was implemented as an analog circuit to reduce the tasks at the main processing unit. The focal plane array represents the photodetector cells while the edge detection circuit represents the horizontal cells and the bipolar cells. A digitized circuit was added to produce binary images so that the output of the neuro-OEIC can be connected

to the FPGA directly.

The fabricated EDC chip had a pixel size of 875 x 600 μm^2 while the fabricated UV photodiode array had a pixel size of 250 x 250 μm^2. To have a fill factor of 100%, at least, both should have the same size. Scaling the design rules from 5 to 1 micron will achieve an area of 175 x 120 μm^2, which is sufficiently fit under the photodiode array.

The fabricated UV focal plane array was expected to generate photocurrent in a range of 14.1 fA - 14.1 nA. However, the fabricated EDC chip with a selected V_{TH} of 2.2 V had a working range of 100 nA - 50 μA. Adding an amplifier with an amplification of around 5000 times might solve this problem. Despite that, the amplifier circuit will consume a large area. Alternative solutions are to increasing the photodiode area for raising the photocurrent, inserting a lens for increasing the photon flux, or shrinking the silicon diode size for increasing the diode's voltage drop.

The EDC fails to detect the object which occurs at the border of the detection area. However, this issue is confirmed in the simulation result. This is caused by the absence of the resistive network at the pixel located at the border. This issue needs a further investigation whether by adding a resistive network and connecting to a potential can solve the problem.

Chapter 4

Simple moving object detection design using FPGA

4.1 Introduction

Field Programmable Gate Array (FPGA) devices are fabricated integrated circuit devices but they are not ready to use. In an FPGA device, the field of gate array is waiting to be connected based on our design. Basically, an FPGA device is used to implement a digital circuit. An FPGA consists of Configurable Logic Blocks (CLBs), Input Output Blocks (IOBs) and Programmable Switch Matrices (PSMs), as shown in Figure 4.1. The CLBs can be seen as a field of gates where our design is implemented. The IOBs serve as the interface from inside of the FPGA chip to the real world. The PSMs connect between CLBs and/or IOBs according to our design. Comparing to an application specific integrated circuit (ASIC), an FPGA device offers re-programmability feature, meaning that we can change our implemented design without re-fabricate the device. Figure 4.2 shows the comparison of design flow between ASIC and FPGA.

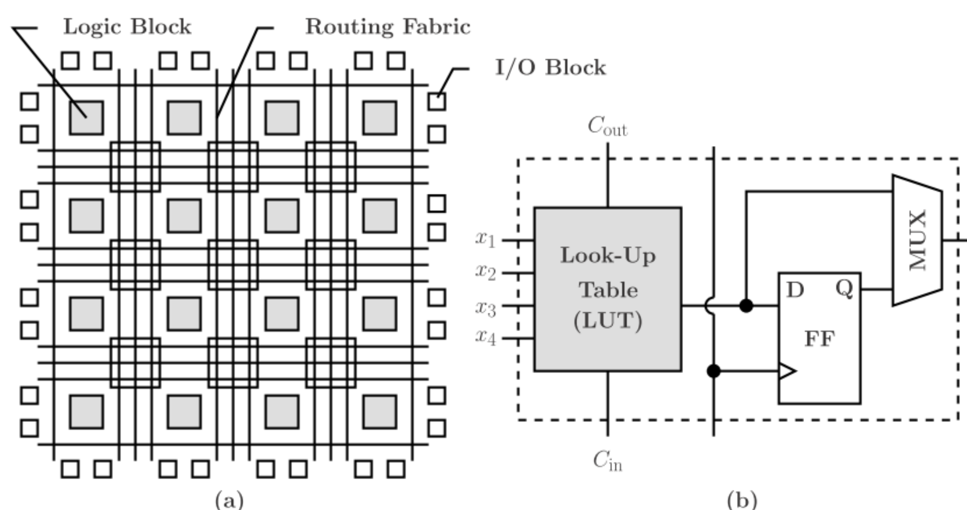


Figure 4.1: An FPGA logic device. (a) Sketch of the FPGA architecture. (b) diagram of a simple logic block [66]

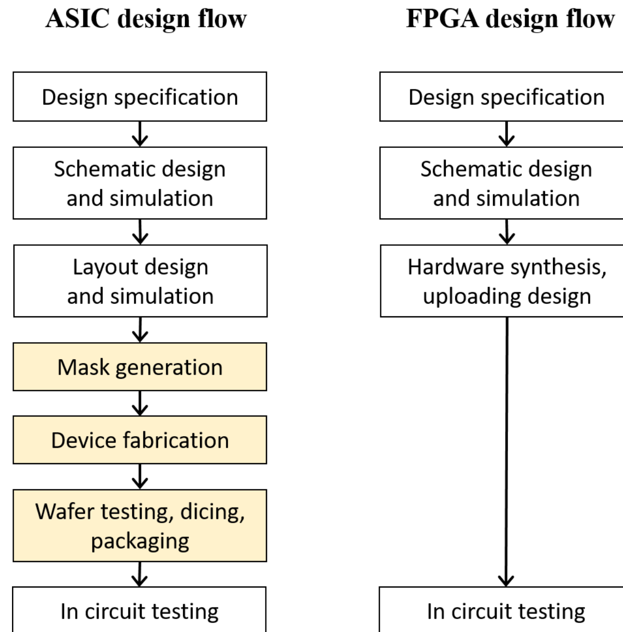


Figure 4.2: Comparison of simplified design flow between ASIC and FPGA

In FPGA, the circuits run in parallel. Therefore, an FPGA device is capable for implementing parallel data processing application. This is the advantage of implementing a circuit in an FPGA, comparing to use microprocessor that runs the instructions sequentially. This chapter describes about the implementation of the moving object detection circuit for two-dimensional array and one-dimensional array. First, the implementation schemes are explained. Second, the moving object detection algorithm is introduced. Third, the design of the implemented circuits are presented. Finally, the conclusion and further development are discussed.

4.2 Implementation schemes

The FPGA is used to process the binary images coming from the edge detection circuit. As described in the design concept in Chapter 1, the ideal case is that the binary images are connected directly to the FPGA's registers pixel-by-pixel. Considering that direct connection from the edge detection circuit and the FPGA's registers can not be actualized in the laboratory at this stage, then there are two options to realize our concept. The first option is, connecting each output of edge detection circuit to the FPGA's input pin. However, this is impossible due to the limitation of the available number of FPGA's input pins. XuLA2-LX25 development board from XESS Corp. was used to implement the moving object detection circuit. This development board has 33 input/output

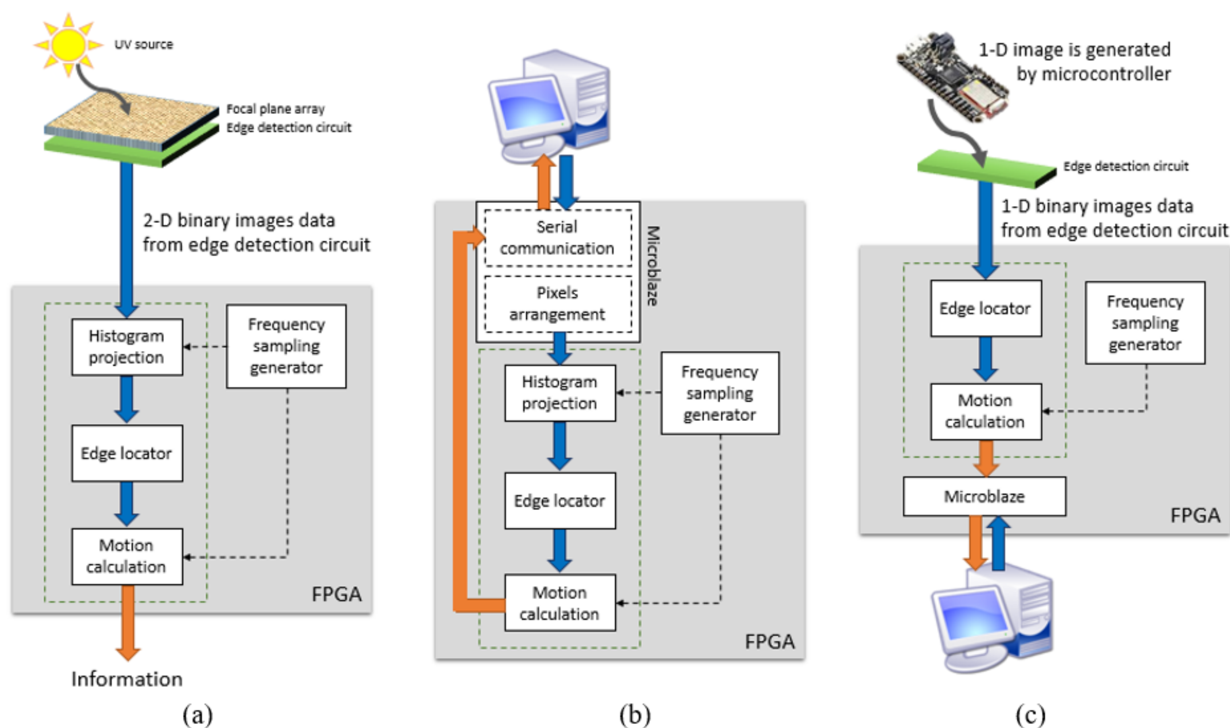


Figure 4.3: Implementation schemes. (a) Proposed connection between the OEIC and the FPGA. (b) Testing the circuit inside the FPGA. (c) Demonstrating of one-dimensional focal plane array

(I/O) pins only, therefore the first option is not suitable to be implemented. The second option is by demonstrating one-dimensional focal plane array. In this thesis work, an edge detection circuit of 1 x 16 pixels was realized, hence it can be connected directly to the FPGA development board.

Figure 4.3 shows the schemes of the FPGA implementation. Ideally, Figure 4.3 (a) is realized as a package of a smart ultraviolet sensor. It connects the OEIC (focal plane array and edge detection circuit) to the FPGA directly, and the FPGA outputs the information. To measure the performance of the circuit inside the FPGA, the scheme as shown in Figure 4.3 (b) is performed. This scheme is used to describe how the motion object detection circuit works in this chapter. A personal computer (PC) generated binary images of 250 x 250 pixels, each row of the generated image was encoded, sent the encoded rows one by one into the FPGA, and read the result from the FPGA back to be stored in a log file for further analysis. Meanwhile, Figure 4.3 (c) is used to demonstrate the concept where the fabricated edge detection circuit chip of 1 x 16 pixels is connected to the FPGA. The microcontroller was used to simulate the photocurrents generated by the focal plane array. A PC in the third scheme was used to record the result for further analysis. When dealing with a PC, a Microblaze, which is a soft processor implemented in the FPGA for controlling the data flow between the FPGA and the PC, is added. The main circuit in the FPGA consists of a histogram

projection, an edge locator, and a motion calculation. The histogram projection circuit in the third scheme was omitted because the received data is already in one-dimensional image. A frequency sampling generator provides a timing to calculate the speed since the unit of calculated speed is pixel/second.

4.3 Histogram projection

The idea of an optical flow algorithm in the computer vision field is to find the similar points between two consecutive images. Therefore, optical flow can be used to measure the motion of the moving object inside the frames. Figure 4.4 illustrates the principle of an optical flow algorithm. There are 3 consecutive frames with dark pixels as object and bright pixel as background. For each 2 consecutive frames, the optical flow calculates the motion vector of each pixel. The pixel motion vector is represented by an arrow in which the length of the arrow shows the distance of how far the corresponding pixel was moved and the arrow's heading shows in what direction the pixel was moved. Inside the object, the optical flow can not tell where the pixels were moved, hence there is no arrow inside it. However, since the optical flow algorithm calculates each pixel motion in a frame, the execution time may take longer. Moreover, within an object, the optical flow algorithm

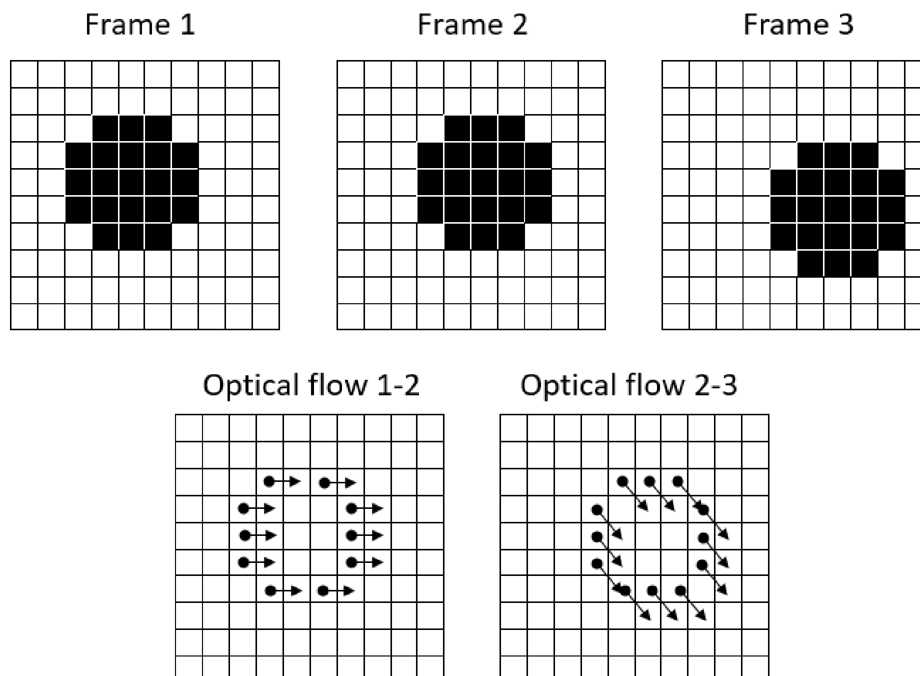


Figure 4.4: Optical flow for 3 consecutive frames at 10 x 10 pixels

produces motion vectors. Determining the actual object motion is by averaging all motion vectors.

In this thesis, a simplify method was utilized. Instead of calculating each pixel in a frame and taking the average, a centroid (center of object) method was implemented. The position of the center of object was obtained in three steps. Firstly, the object is projected vertically and horizontally. Next, the edge position of the projected image is located. We called the starting and ending of the projected image as edges. Finally, the centroid is calculated from the edge positions. In the first step, it works like a histogram projection algorithm. A histogram projection algorithm accumulates the number of pixel in the rows as well as in the columns. Accumulating means that adder circuits are required. For an image with m x n pixels, it would take m x n adder circuits to perform the projection at a time which consumes a huge FPGA resources. In this case, since the image is in binary and the object area will be defined as a square, it is not necessary to count the number of the pixel. The system only need an information whether an object exists in a row or in a column. Therefore, logical ORs was applied for each row and column to substitute the adder circuits. Using this way, the FPGA resources was reduced significantly. Figure 4.5 illustrates the process of the histogram projection at 10 x 10 pixels array. Figure 4.5 (a) shows the original histogram projection algorithm in the computer vision field, where the projected values are the summation of corresponding row or column. While Figure 4.5 (b) shows the replacement of adders with OR-gates, in which the projected registers only have a binary value. Hence, we called it as a binary histogram projection. The image registers receive the binary images from the edge detection circuit. Within the image registers, the bright pixels show the background and the dark pixels indicate the object.

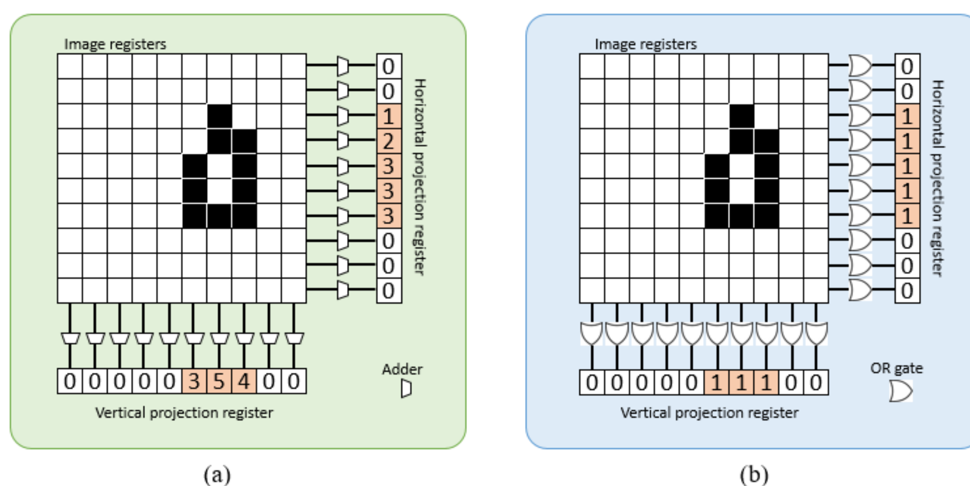


Figure 4.5: Histogram projection. (a) Original algorithm. (b) Modified algorithm

4.4 Circuit design

A motion detection circuit for an image with 250 x 250 pixels was implemented in the FPGA. [67] The circuit mainly consists of four sub-circuits which are the binary histogram projection, the edge locator, the motion calculation, and the frequency counter. Those circuits were written using very high-speed hardware description language (VHDL) within Xilinx ISE Webpack 14.5 Integrated Development Environment (IDE). To receive data stream from the PC and to send the calculation result back to the PC, a soft-processor named Microblaze was added in the FPGA side. The Microblaze was developed using Xilinx Software Development Kit which is integrated with ISE Webpack IDE. The instruction for the Microblaze processor was written in C++ language. At the PC side, a software written in Processing 2.2.1 was designed to generate a two-dimensional image with a moving object inside the image. The Processing software offers simple instructions to access the serial ports of the PC. Figure 4.6 shows the system block diagram to examine the implemented algorithm in the FPGA.

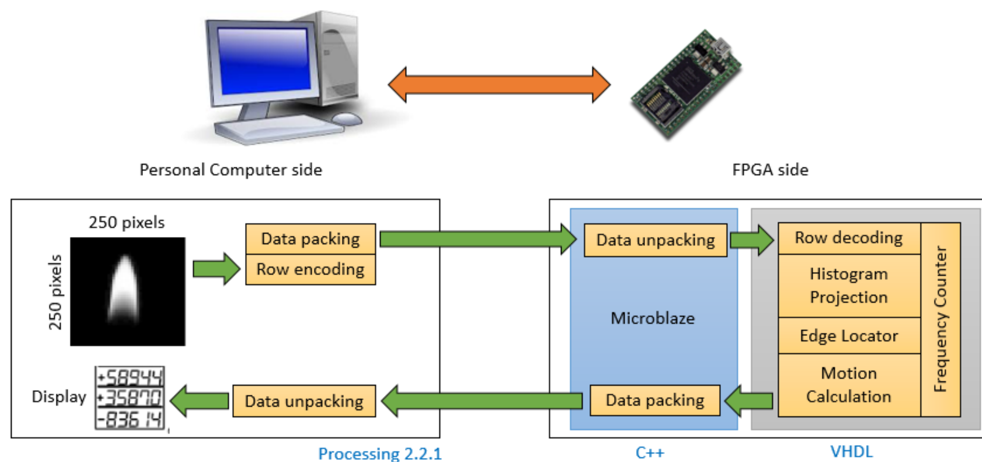


Figure 4.6: System block diagram

Sending a binary image of 250 x 250 pixels would cost 7,832 bytes. To reduce the time for sending the binary image, the image is compressed in advance. The illustration of compressing the binary image is shown in Figure 4.7. Each row of the binary image is encoded into two bytes which are the start position and the length of the object in the corresponding row. A byte stores an integer number between 0 to 255. Finally, the compressed row information is wrapped with a start byte (255) and a stop byte (254) for synchronizing purpose at the receiver side. Therefore, a binary image of 250 x 250 pixels is compressed into 502 bytes. In other words, the amount of data to be sent has a significant reduction as much as 93.6%.

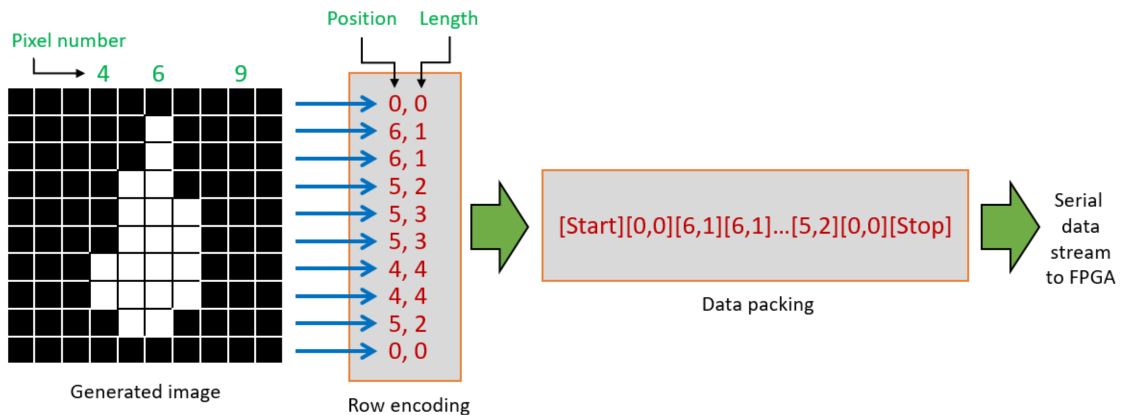


Figure 4.7: Steps of compressing the two-dimensional image

In the FPGA side, the data streams coming from the PC are received by the Microblaze. The Microblaze is responsible to unpack the incoming data also to generate a signal to trigger the next sub-circuit. The next sub-circuit is a row shifter which the schematic symbol is shown in Figure 4.8. The row shifter circuit receives 8-bit data of the object's start position and 8-bit data of the object's length in a corresponding row. This information is expanded to 250-bits data which represents the original row of the generated image, then is saved into the image registers. To reduce the register consumption in the FPGA, the image registers size is only for one row of 250-bits instead of saving a whole binary image of 250 x 250 bits. Taking the advantage of the data that comes row-by-row, the content of the image register will be replaced by the new data, while the projection registers update their content accordingly, as shown in Figure 4.9.

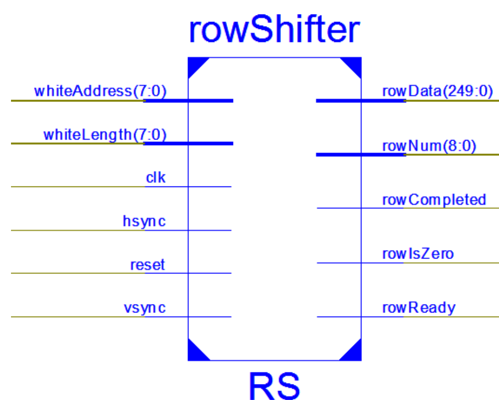


Figure 4.8: Schematic symbol of the row decoder

The schematic symbol of the histogram projection sub-circuit is shown in Figure 4.9 (a). Figure 4.9 (b) and Figure 4.9 (c) show the update mechanism of the horizontal projection registers and the vertical projection registers, respectively. The horizontal projection registers updates its

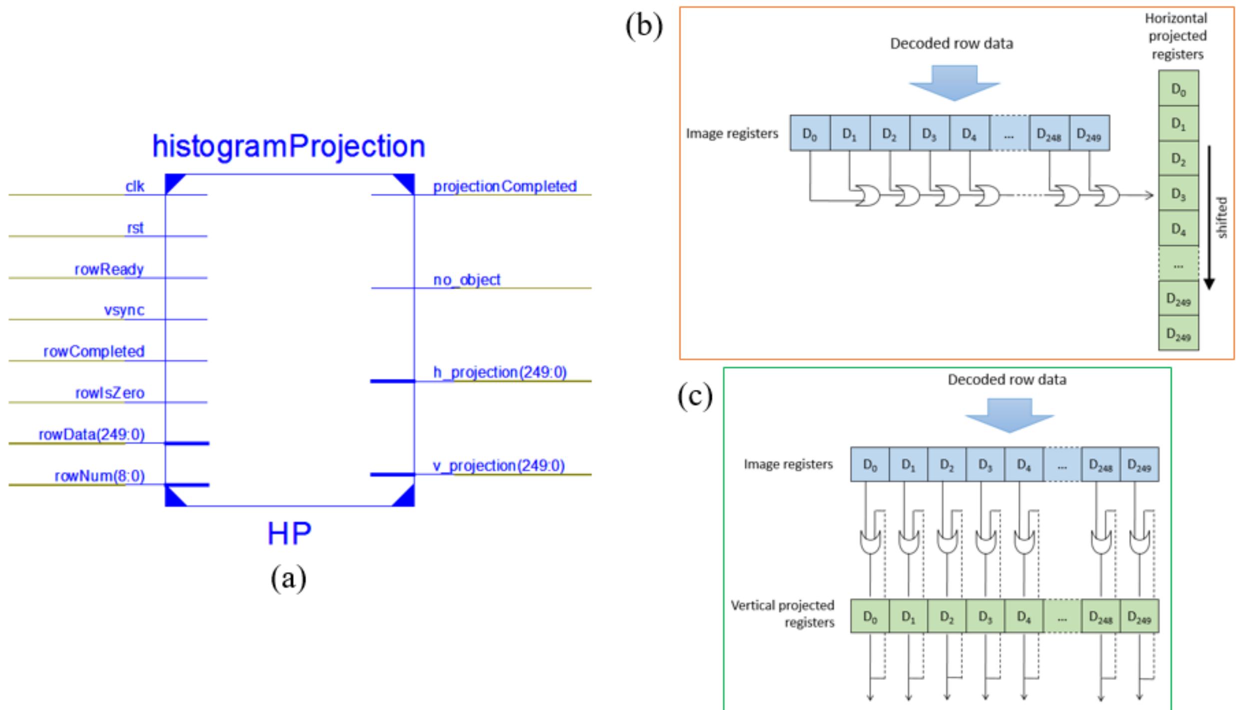


Figure 4.9: Histogram projection sub-circuit. (a) The schematic symbol. (b) The horizontal projection mechanism. (c) The vertical projection mechanism

registers bit-by-bit by doing the logic-OR to the whole image registers' content for each incoming decoded row data. The vertical projection registers update its whole registers by doing the logic-OR between image registers' content and its previous value for each incoming decoded row data.

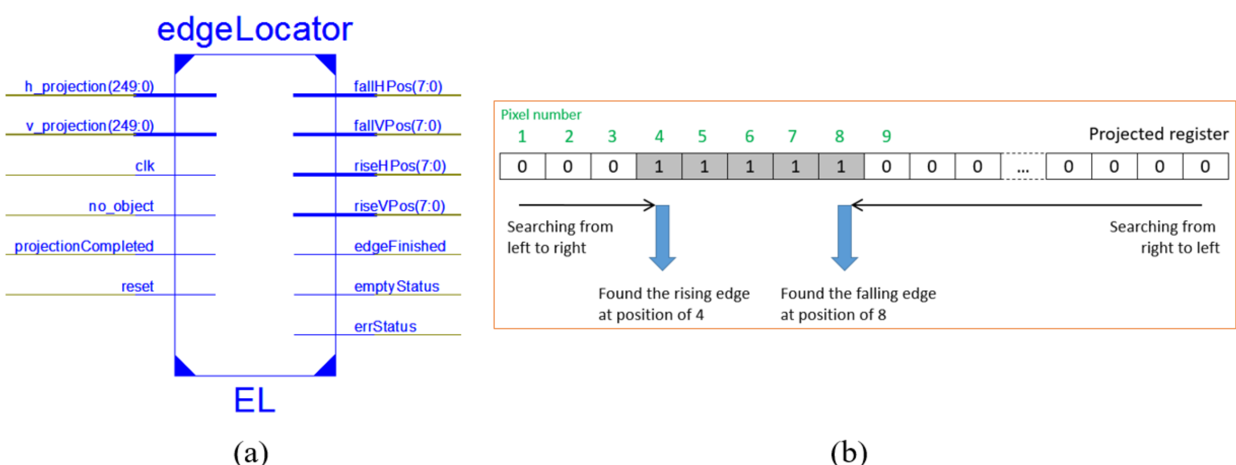


Figure 4.10: Edge locator sub-circuit. (a) The schematic symbol. (b) The searching algorithm

Next, the edge locator sub-circuit searches the edge position in each of the projection registers.

The schematic symbol and the searching algorithm of the edge locator sub-circuit is shown in Figure 4.10. The algorithm searches from the most left side of the projected registers and moves to the right side bit-per-bit. When the value of the projected registers is “1” (which corresponds to the object), the searching process stops and marks the number of steps as the rising edge location. After that, the algorithm continues to search from the most right side of the projection registers and moves to the left side bit-per-bit. Again, when the value of the projected registers is “1”, the searching process stops and marks the number of steps as the falling edge location. The searching algorithm is applied for both vertical projected register and horizontal projected register. Figure 4.10 (b) shows the example of the searching algorithm. The series of logic-1 indicates the object which represents the hydrogen flame in a particular row. The first searching process found that the pixel number 4 is indicated as the rising edge location of the object in that row. Then, the second searching process found that the pixel number 8 is indicated as the falling edge location of the object in that row. It is also designed that when the first searching process cannot find the object in a given row then the algorithm generates an empty status and cancels the second searching process. The information of the edge locations are used for the next sub-circuit which is the motion calculator. Those four edge locations are the rising edge vertical (RV), the falling edge vertical (FV), the rising edge horizontal (RH), and the falling edge horizontal (FH).

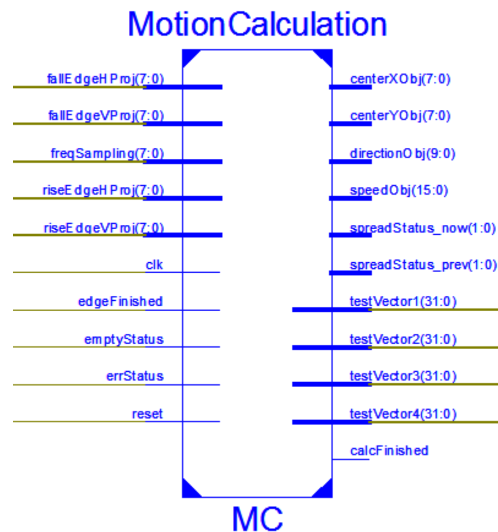


Figure 4.11: Schematic symbol of motion calculator

The motion calculator sub-circuit computes the edge locations of the object into some information including the object location, the object speed, the object direction, the object size, and the spreading status of the object. The object locations (OX and OY) are defined as a midpoint of the histogram projection, as shown in eq. 4.1 and eq. 4.2. The unit of the object location is pixel.

$$OX = \frac{1}{2}(RV + FV) \tag{4.1}$$

$$OY = \frac{1}{2}(RH + FH) \tag{4.2}$$

The object velocity is defined as the change of the displacement between two consecutive images, as illustrated in Figure 4.12. The index n means the current image, the index $n-1$ means the previous image, and T means the time interval between two consecutive images. The object velocity in the x-direction and in the y-direction are defined as in eq. 4.3 and eq. 4.4, respectively. Thus, the object speed (OP) is defined as a resultant of the object velocities (VX and VY), as shown in eq. 4.5. The unit of the object velocity and the object speed is pixel/s.

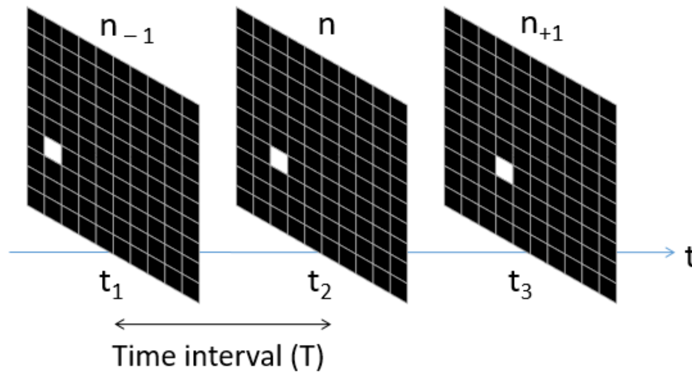


Figure 4.12: Defining the speed of a moving object

$$VX = (OX_n - OX_{n-1})/T \tag{4.3}$$

$$VY = (OY_n - OY_{n-1})/T \tag{4.4}$$

$$OP = \sqrt{(VX^2 + VY^2)} \tag{4.5}$$

The object direction (OD) is defined as an inverse tangent of its velocities, as shown in eq. 4.6. The unit of the object direction is degree.

$$OD = tan^{-1}(VY/VX) \tag{4.6}$$

The object size (OZ) is defined as a product of the lengths of the histogram projection, as shown in eq. 4.7. The unit of the object size is pixel^2. The maximum value of the object size is equal to its square area. By comparing the object size between two consecutive images, the spreading status determines whether the object becomes bigger, smaller, unchanged, or disappear from the image.

$$OZ = (FV - RV + 1) \times (FH - RH + 1) \tag{4.7}$$

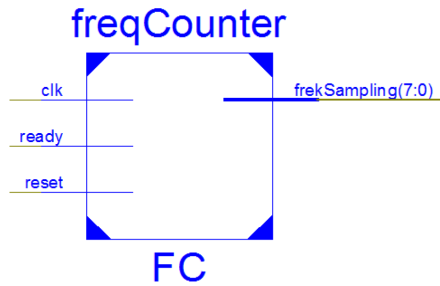


Figure 4.13: Schematic symbol of the frequency counter

The frequency counter sub-circuit works by counting the number of event that occurs at a duration of one second. The event is triggered when the binary image of 250 x 250 pixels is transferred completely. In this circuit, the averaging is performed for eight times of counting, as shown in eq. 4.8, where FS_n is the frequency sampling counting result. The index $n = 0$ means the current reading value. The averaging reason is to produce a stable reading value. This value is used to calculate the object velocity for the T parameter.

$$\frac{1}{T} = \frac{1}{8} \sum_{n=-7}^{0} FS_n \tag{4.8}$$

The calculation result from the motion calculator circuit is sent back to the PC. In the PC side, the calculation result is displayed and saved in a log file for further analysis. The schematic of the motion object detection with the interconnection of the sub-circuits is shown in Figure 4.14. There are three additional sub-circuits added in this design. First, the microblaze1 sub-circuit is the Microblaze soft-processor provided by the library of the ISE Webpack IDE. Second, the sub-circuit labeled oneShot4Sync is designed to synchronize the signal pulse with the internal clock. Third, the ClkGen sub-circuit multiplies the external clock of 12 MHz into the system clock of 100 MHz which is used for ticking the whole circuits.

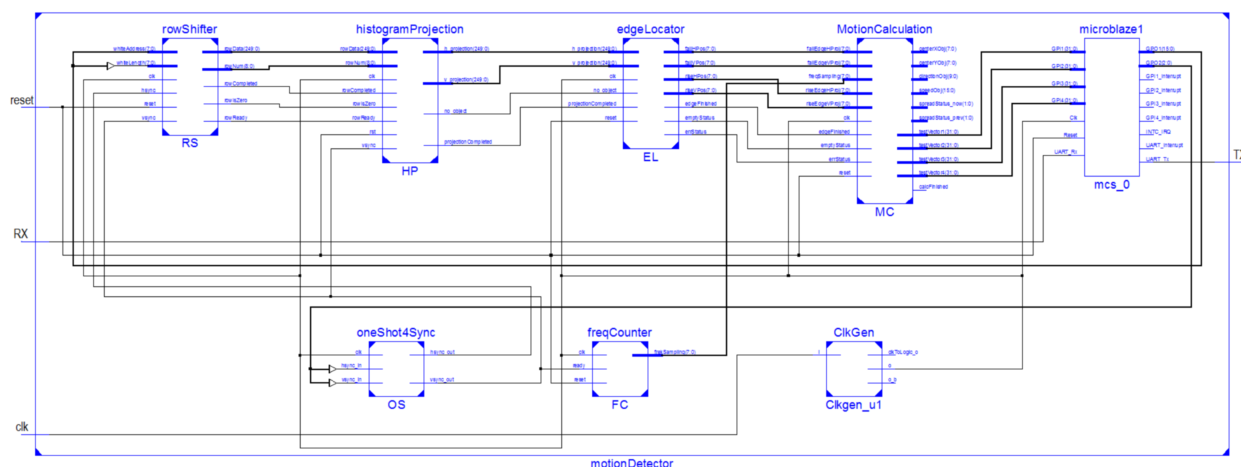


Figure 4.14: Schematic of the motion object detection

4.5 Implementation result

The performance of the motion object detection circuit was evaluated in three ways. First, an object moved constantly at a low speed of 71 pixels/s. Second, an object moved constantly at a high speed of 3,551.14 pixel/s. Third, an object rotated constantly at a speed of 12.4 rad/s.

Figure 4.15 shows the experiment result of the low-speed testing of an object with a circle-shape which moved from the left to the right in the image frame of 250 x 250 pixels. The origin (the coordinate of 0,0) of the image frame is at top left coordinates. The object was programmed to move with a speed of 71 pixels/s, a direction of 0°, a diameter of 10 pixels, and a y-position of 128. The object was designed to appear in the image, to move to the right side, and then to disappear from the image. From the Figure 4.15, the x-position of the object (OX) increased linearly from 0 to 249, meaning that the object moved from the left side to the right side. The size of the object (OZ) changed gradually from 0 to 100 pixel^2, then become a constant at 100 pixel^2, and finally decreased gradually become 0 pixel^2. This explains that, first, the object was not inside the image frame, then gradually appeared and moved with a constant size, and finally disappeared from the image frame. The speed of th object (OP) was also detected at a constant value of 71 pixels/s. The vibrations at the beginning and at the end indicates that, at the beginning, the size of the object gradually increased. Sometimes, the calculated value of the x-position of the object was constant. Thus, the calculated speed result was zero. This also happened when the object gradually disappeared from the image frame.

Figure 4.16 shows the experiment result of the high-speed testing of an object with a circle-shape in a diameter of 10 pixels which moved from left to right in the image frame of 250 x 250

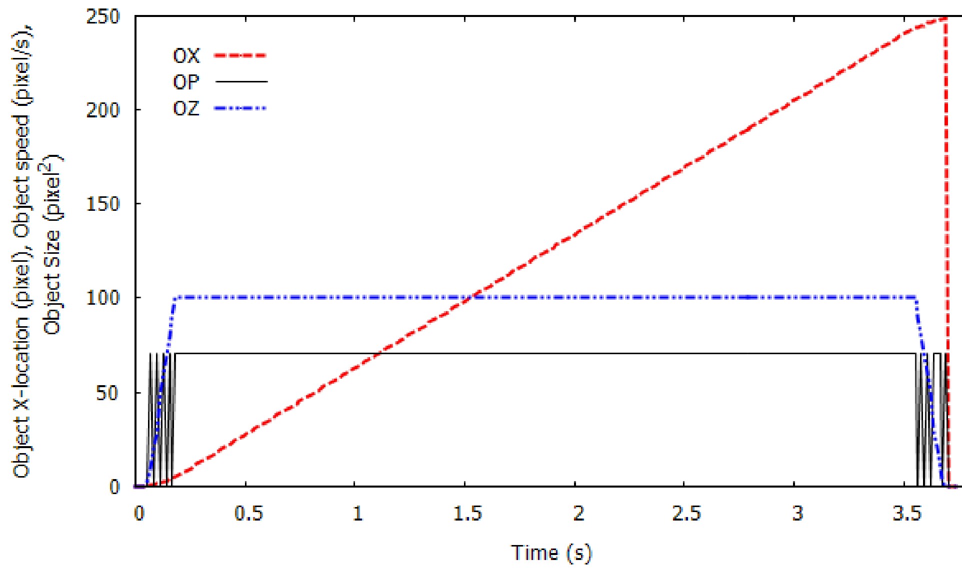


Figure 4.15: The result of the object moved constantly at 71 pixels/s

pixels. The object had a speed of 3,551.14 pixels/s, a direction of 0°, and a y-position of 128. The x-position of the object (OX) confirms that the object was moved from the left to the right in the image frame. The size of the object (OZ) also confirms that the object was moved across the image frame. The speed of the object (OP) was measured at 3,551 pixels/s when the object was close to the center of the image frame.

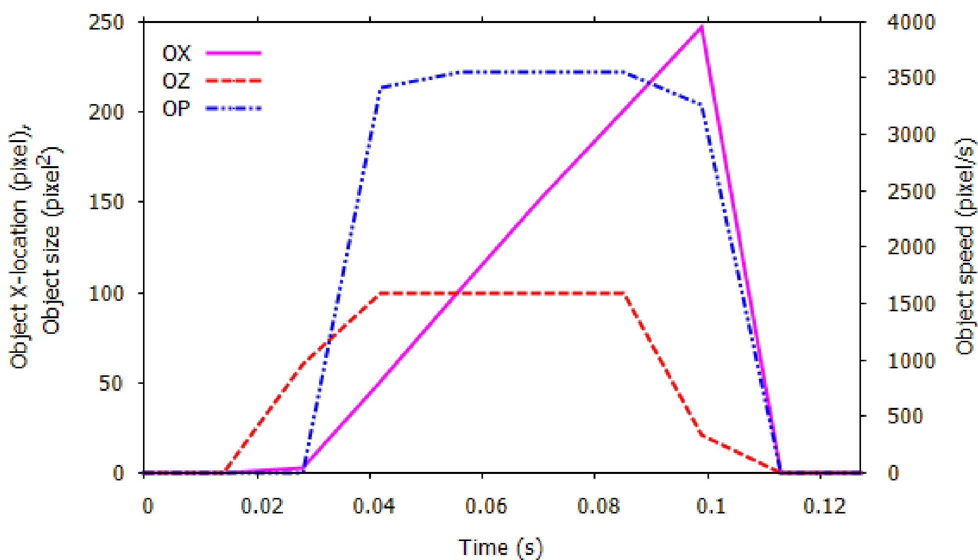


Figure 4.16: The result of the object moved constantly at 3,551,14 pixels/s

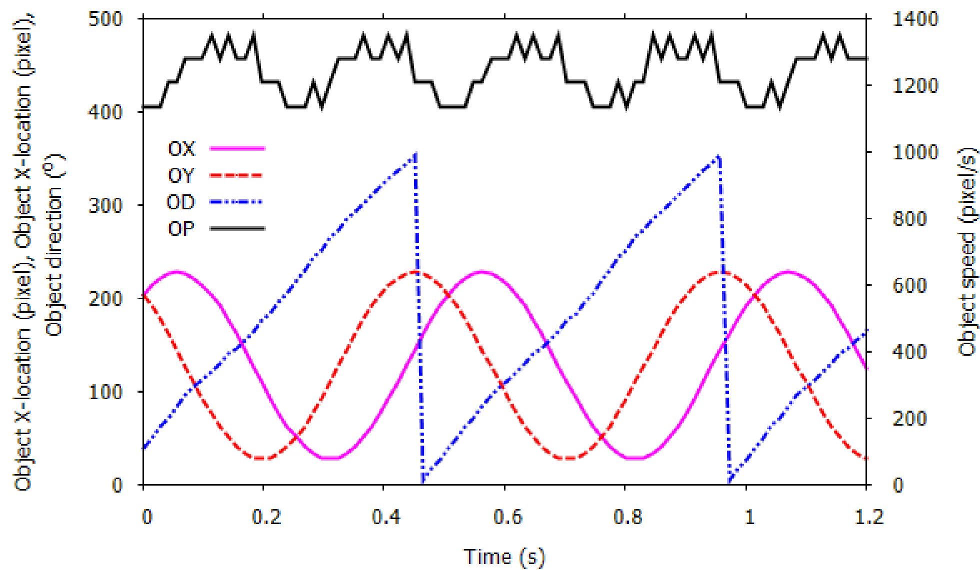


Figure 4.17: The result of the object rotated constantly at 12.4 rad/s

Figure 4.17 describes the experimental results of the direction testing. An object with a circle-shape in a diameter of 10 pixels moved in a circular loop at an angular speed of 12.4 rad/s (or 710.5 °/s). The center position of the object (defined by OX and OY) was rotating and appeared as a sinusoidal pattern in the graph. The measured direction (OD) appeared as a sawtooth pattern from around 6° to 353°. This means the system can measure the direction of the object, but the speed of the object (OP) was not measured correctly because the system implemented a linear speed calculation. These experimental results confirm that the FPGA was able to analyze a given moving object.

The implemented system in the FPGA consumed 30% of available slices (1,132 of 3,758 slices). The real-time performance using a PC with Intel® Core™i3-4130 CPU and 4GB RAMs is 71 frames/s or 14.08 ms. The implemented circuit in the FPGA took about 7.05 ms to process one binary image at a clock rate of 100 MHz. The process for receiving a complete binary image of 250 x 250 pixels from the PC was 7 ms with a serial communication speed of 921,600 bit per second (bps), while the remaining processes (the histogram projection, the edge locator, and the motion calculation) consumed about 0.05 ms.

4.6 Scaling of the image resolution

From the experiments, the motion object detection circuit in the FPGA executes each image frame of 250 x 250 pixels at 50 μs. This gives a processing time of up to 20,000 frames/s. Nevertheless, one should consider about the relationship between the frame rate and the speed of the object. Higher frame rates would be useless for slow moving objects, and vice versa. Theoretically, the range of detectable speeds can be derived from Figure 4.12. The relation between the image size and the time interval between two consecutive frames to get the range of detectable speeds is shown in eq. 4.9.

$$V_{min/max}(pixel/s) = D_{min/max}(pixel)/T(s) \tag{4.9}$$

where $V_{min/max}$ is the range of detectable speed, $D_{min/max}$ is the smallest and the largest displacement of the object in the image frame, and T is the time interval between two consecutive frames. This thesis work uses a unit of the speed in pixel/s. A calibration should be conducted for unit conversion from pixel/s to m/s, as an example. The hydrogen flame might have a speed of 18.6 m/s. [68] After conducted a calibration, one can determine the appropriate frame rate.

Realizing the parallel data transfer between the OEIC and the FPGA by stacking both of them means the time for transferring the images from the OEIC into the FPGA is very short or at least it only need a single clock period. The question about what will happen if the image resolution increases might arise. In this case, when the image resolution is increased, the histogram projection circuit and the edge locator circuit will be scaled. Meanwhile, the motion calculation circuit is unchanged. It means that the system execution time would not be scaled for transferring the images from the OEIC to the FPGA (in case the stacking can be realized) and also for the calculation circuit. Here, the row shifter circuit is excluded by assuming that the image register inside the FPGA is enough to handle, as illustrated in Figure 4.5. The histogram projection circuit utilizes OR gates for both vertical projection and horizontal projection. The execution time of the histogram projection circuit ($t_{HP}(m,n)$) is assigned by the longest propagation delay (t_{PD}) of the OR gates as defined in eq. 4.10.

$$t_{HP}(m,n) = (h-1) \times t_{PD} \tag{4.10}$$

where h = *max*(m,n), m is the number of row, and n is the number of column. A minus one is added because the last OR gate is connected to the last two pixels. In other words, an (n)-number of

row/column requires $(n-1)$-number of OR gates. The edge locator circuit searching the logic-1 within the projected registers from the left to the right, step by step. If the logic 1 is found then it seeks again from the right to the left, step by step. When the logic-1 is found, the number of steps is equal to the position of the edge. Therefore, the execution time of the edge locator circuit ($t_{EL}(m,n)$) is defined by eq. 4.11.

$$t_{EL}(m,n) = [(m+2-dV)+(n+2-dH)] \times t_{CLK} \tag{4.11}$$

where dV is the length of the vertical projected, dH is the length of the horizontal projected, and t_{CLK} is the system clock period of the FPGA. Hence, the total execution time of the circuit ($t_{CIR}(m,n)$) in the FPGA is defined by eq. 4.12.

$$t_{CIR}(m,n) = t_{HP}(m,n) + t_{EL}(m,n) + t_{FIX} \tag{4.12}$$

where t_{FIX} is the execution time of the calculation circuit and the logics for controlling those circuits. The value of t_{FIX} is not scaled with the higher-resolution images because their circuit remains unchanged.

Ideally, only a single object is allowed to appear in the image. When more than one object appears in the image frame, the current system will fail to distinguish which is which. Instead, the current system counts them as one object since the edge locator algorithm only finds the outer of the object. In order to differentiate a multi object, an enhanced object detection algorithm might be implemented in the future.

4.7 Conclusion

A simple moving object detection using a binary histogram projection has been discussed. A high-speed motion object detection of 250 x 250 pixels has been implemented in the FPGA. The design occupied 30% of available slices resources in the FPGA. A PC was used to emulate the output of the OEIC and sent the binary images to the FPGA at the frame rate of 71 frames/s. Therefore, the range of the real-time detectable speeds was 71 pixels/s to 17,685 pixels/s. The execution time of the system was 7.05 ms in which the time for handling the data transfer itself between the PC and the FPGA spent 7 ms. This means, if the parallel data transfer between OEIC and FPGA can be realized in the near future then the time to handle the data transfer between the

OEIC and the FPGA could be neglected and the real-time performance may increase up to 20,000 frames/s.

A question about image resolution scaling has been introduced as well. The scaling of the image resolution affects the execution time of the histogram projection circuit and the edge locator circuit while the execution time of the motion calculation circuit remains the same. The approximation of the system execution time has been described.

The binary histogram projection algorithm may apply best for one object detection. For a multiple objects, the binary histogram projection algorithm has a problem to distinguish the object which is which, mainly due to the object occlusion. When multiple objects occur in the current system, it will be detected as a single object since the current system detects the outer boundary of the objects that appear in the image frame. An enhanced algorithm should be implemented in the future to address this issue.

Chapter 5

Flame speed calculation

5.1 Introduction

The edge detector circuit of 1 x 16 pixels has been fabricated. The motion object detection has been implemented in the FPGA as well. Then, the fabricated edge detection circuit chip was connected to the FPGA using wires to evaluate the flame speed calculation by the FPGA circuit. Since the photodiode array is under development stage, the photocurrent was simulated by using a microcontroller. The microcontroller was programmed to generate patterns as a moving object.

This chapter describes about the evaluation of the speed calculation by the motion object detection circuit in the FPGA in which the FPGA receives the binary image from the fabricated edge detector circuit chip. First, the experimental setup and the measurement result of the object's speed are presented. Next, the system is extended to calculate the flame speed with a spurt model, since the previous model described in Chapter 4 is not represented a realistic model of the hydrogen flame. Finally, the conclusion and further development are discussed.

5.2 Experimental setup and measurement result

Figure 5.1 shows the experimental setup by wired-integrating the fabricated EDC chip and the FPGA. The microcontroller was used to generate moving patterns. The output pins of the microcontroller produce 3.3 V for the logic-1. The silicon diode in the EDC chip has a forward voltage of 0.58 V. The V_{DD} and V_{TH} was 2.2 V and 5.0 V, respectively. It was expected that the current of 5.2 μA will flow into the EDC chip's inputs by placing 100 kΩ resistor between them. The LEDs were used to give a direct visual observation. The PC was applied to select the sampling frequency generated by the frequency generator circuit in the FPGA. The PC also displayed the information sent by the motion object detection circuit in the FPGA and saved the information as files for further analysis.

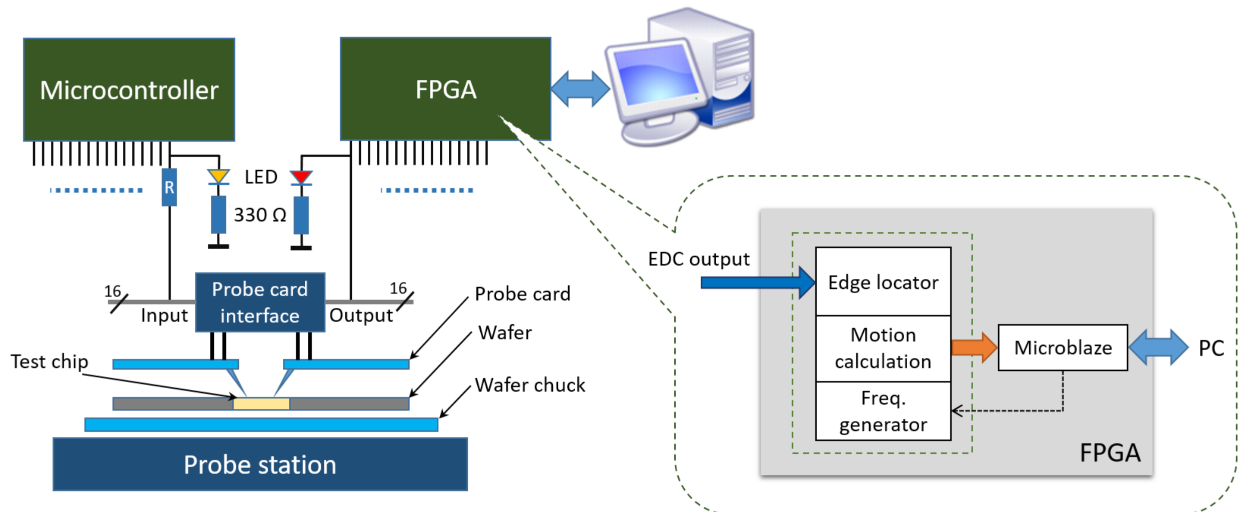


Figure 5.1: Integration set-up between EDC chip (as the test chip) and FPGA

The motion object detection circuit inside the FPGA has been modified to receive binary images with a size of 1 x 16 pixels, instead of 250 x 250 pixels as described in Chapter 4. The motion object detection circuit produces information about the centroid, size, centroid's speed, centroid's direction, and spreading status of the object. The information has a width of 72-bit (9 bytes), as shown in Figure 5.2. The information consists of 8-bit for the centroid of the object, 4-bit for the size of the object, 16-bit for the speed of the object's centroid, 8-bit for the direction of the object's centroid, 4-bit for the spreading status of the object, 8-bit of the selected sampling frequency of the system, 8-bit for the checksum, 8-bit for the timestamp, and 8-bit for the synchronization. The selected sampling frequency was sent back to the PC as a feedback to the user. The checksum, timestamp, and synchronization were used for maintaining the data integrity. The information from the FPGA was sent to the PC via universal asynchronous receiver/transmitter (UART) serial communication at a rate of 460,800 bit per second (bps). Sending a data of 9 bytes (1 byte data will be wrapped by UART as 10-bit that contains 8-bit data, 1 start-bit, and 1 stop-bit) at 460,800 bps takes about 0.195 ms or about 5,120 s^{-1}. This means that the speed of the moving pattern from the microcontroller should not exceed 5,120 pixel/s to maintain the continuity of the receiving information generated by the FPGA. Therefore, the microcontroller was programmed to generate a moving pattern with a speed of 44 pixels/s until 2,049 pixel/s.

The motion object detection circuit in the FPGA calculates the speed of the object by multiplying the displacement of the object between two consecutive frames with the sampling frequency, as described in Chapter 4. At the beginning of each measurement, the PC informs the FPGA to select the desired sampling frequency generated by the circuit in the FPGA. The information about the value of the generated sampling frequency from the FPGA is sent back to the PC. Figure 5.3

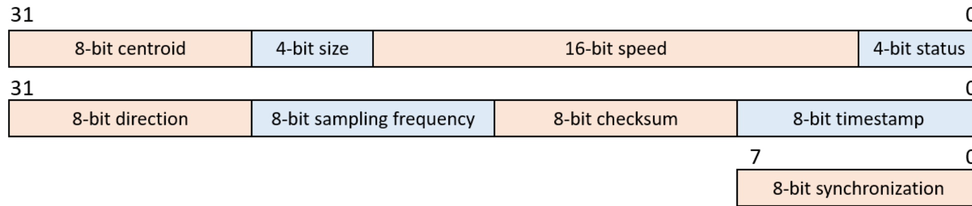


Figure 5.2: The information generated by the FPGA for one-dimensional array of 1 x 16 pixels

shows the result of the speed reading at a given input speed with the sampling frequency of 10 Hz and the size of the object was set to 1 pixel. For a particular input speed, the maximum and the minimum values of the measurement speed are plotted in the graph. As we can see in Figure 5.3, the system failed to measure the object with a speed of 164 pixels/s. As described in the Chapter 4, the maximum detectable speed is the number of the pixel times the sampling frequency. This measurement result was performed on a one-dimensional array of 1 x 16 pixels at a sampling frequency of 10 Hz. Therefore, the maximum detectable speed is 160 pixels/s.

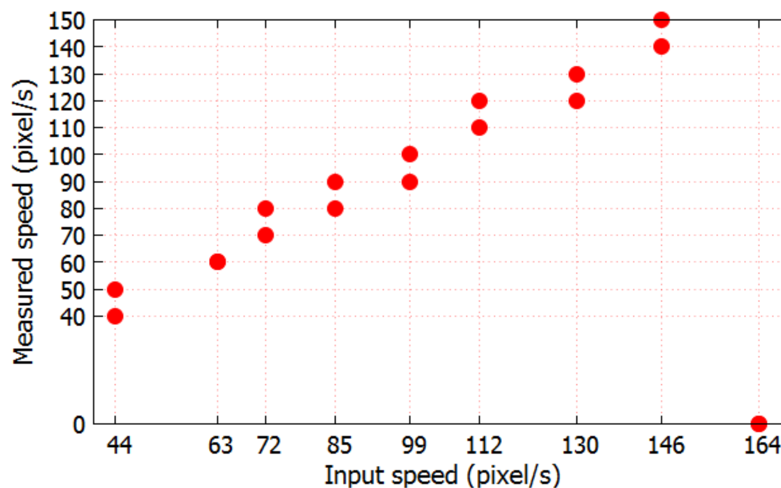


Figure 5.3: The speed measurement at 10 Hz sampling rate

By increasing the sampling frequency to 20 Hz, the object with a speed of 164 pixels/s can be measured by the system. Figure 5.4 shows the result of the speed measurement with the sampling frequency of 10 Hz and 20 Hz. For the sampling frequency of 20 Hz, the system failed to measure the object with a speed of 339 pixel/s Hz. This is because at sampling frequency of 20 Hz, the maximum detectable speed is 320 pixel/s. Figure 5.5 shows the result of the speed measurement with various sampling frequency to measure the speed of the object in a range of 1.7 pixel/s - 2,049 pixel/s. From this graph, it can be concluded that the system is able to detect the speed of the moving object.

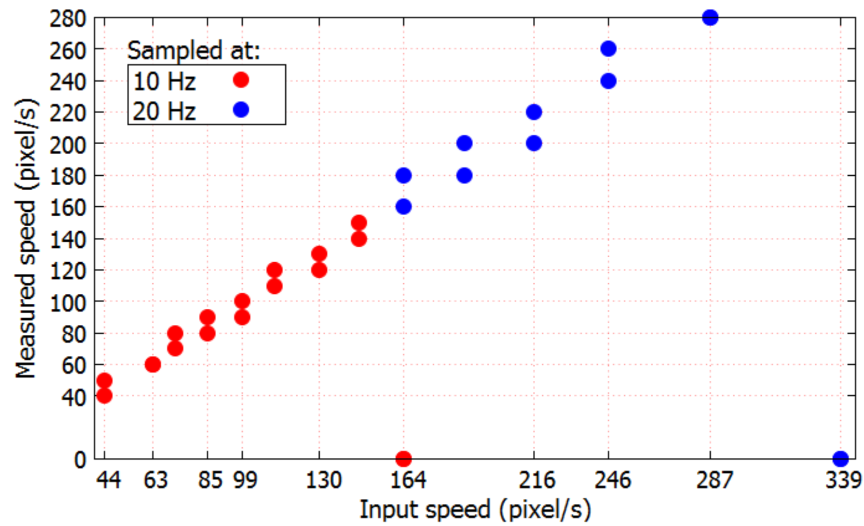


Figure 5.4: The speed measurement at 20 Hz sampling rate

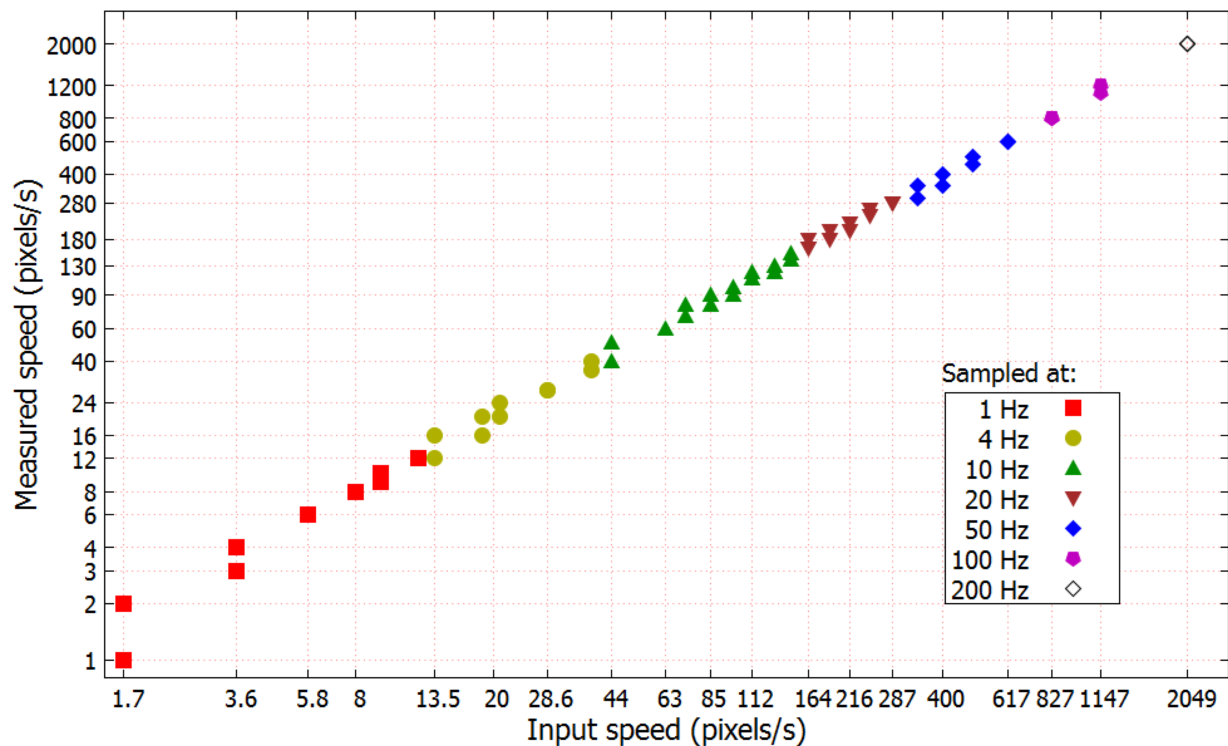


Figure 5.5: The result of the speed measurement

5.3 Flame speed calculation with spurt model

The flame speed is the measured rate of expansion of the flame front in a combustion reaction. One approach of modern combustion theory describes a premixed flame as a thin interface separating

reactants and products. The surface of the interface that faces reactants is often termed as the flame front. Similarly, the surface that faces the products can be termed as the flame back. The flame speed is related to a fixed observer. [68] In this case, the fixed observer is the smart UV sensor.

The smart UV sensor is targeted to capture a hydrogen flame in which the flame source may come from a high-pressure pipe or tank. In this case, the hydrogen flame might form as a spurt as shown in Figure 5.6. The series of formation might happen as follows. The flame starts to ignite from the leakage source. Next, the flame expands rapidly. Then, the flame's size stays steady for a moment. After the pressure or the hydrogen concentration in the pipe or tank decreases, the flame size shrinks. Thus, there are five phases of the flame, namely appear, expand, steady, shrink, and disappear. To simplify the calculation, the flame is considered as a rectangular shape as shown in Figure 5.7. The flame speed is defined from a rectangle's side which has the largest displacement value relative to the ignition point.

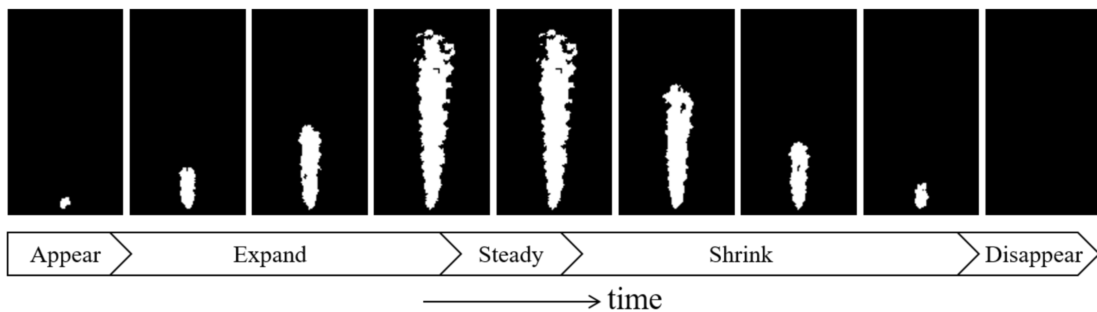


Figure 5.6: Hydrogen flame as a spurt

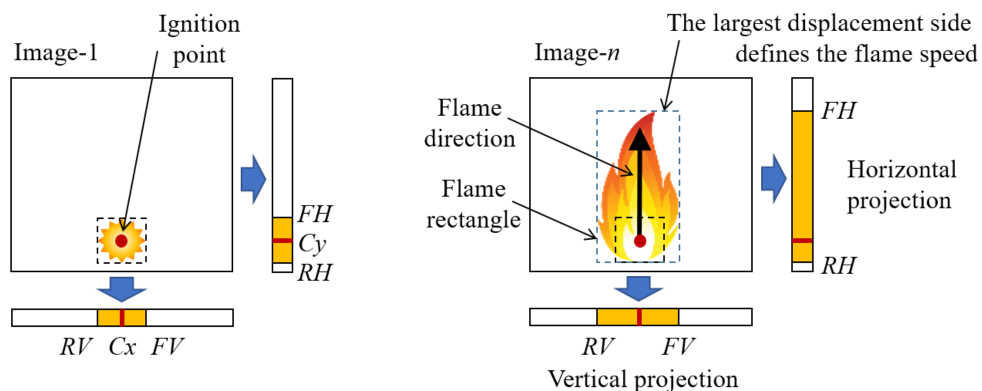


Figure 5.7: Flame speed definition

When the flame object is appear in the image, the system locates the centroid of the object

using the projected image. The first centroid (C_X, C_Y) appeared in the image is assumed as the ignition point of the flame. As the flame expands, the system tracks the displacement of each rectangle's side relative to the ignition point. When the system detects that the flame shrinks, the system decides which rectangle's side has the largest displacement. Then, the flame speed is defined from the largest displacement divided by the elapsed time counter. The elapsed time is generated by a dedicated counter that has a 100 μs base clock. The elapsed time counter is started when the spreading status identifies the appear phase. When the shrink phase is detected by the system, the elapsed time counter is stopped. The elapsed time counter is reset when the disappear phase is obtained. Figure 5.8 shows the block diagram of the generated information. The value of the light blue-filled rectangles are sent from the FPGA out.

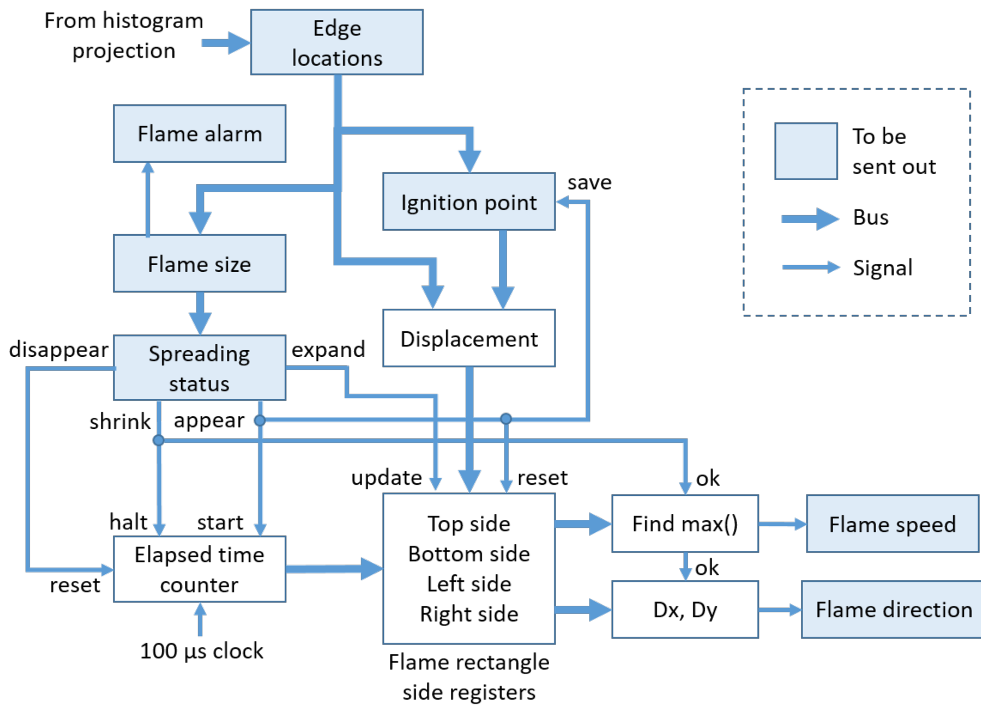


Figure 5.8: Block diagram of the generated information

The ignition points (C_X and C_Y) are calculated similar with eq. 4.1 and eq. 4.2, as shown in eq. 5.1 and eq. 5.2, respectively.

$$C_X = \frac{1}{2}(RV + FV) \tag{5.1}$$

$$C_Y = \frac{1}{2}(RH + FH) \tag{5.2}$$

Here, RV, FV, RH, and FH are the edge locations of the projection image described in Chapter 4. The flame speed (V_{FS}) is defined as in eq 5.3.

$$V_{FS} = D_{MAX}/T_{elapsed} \tag{5.3}$$

Here, D_{MAX} is the largest displacement of the rectangle's side of the flame which is defined as shown in eq. 5.4 and $T_{elapsed}$ is the elapsed time from the appear phase until the shrink phase.

$$D_{MAX} = max\{C_X - RV, FV - C_X, C_Y - RH, FH - C_Y\} \tag{5.4}$$

The direction of the flame is calculated using eq. 5.5

$$\theta = tan^{-1}\left(\frac{D_Y}{D_X}\right) \tag{5.5}$$

Here, D_X is the displacement's resultant of the x-axis and D_Y is the displacement's resultant of the y-axis, as shown in eq. 5.6 and eq. 5.7.

$$D_X = (FV - C_X) - (C_X - RV) \tag{5.6}$$

$$D_Y = (C_Y - RH) - (FH - C_Y) \tag{5.7}$$

5.3.1 Two-dimensional array implementation result

The modified motion object detection circuit for calculating the flame speed was implemented in the FPGA. The FPGA circuit was designed to process binary images with a size of 250 x 250 pixels. For testing purpose, the PC was used for generating the binary images with the object to represent the flame. The experimental setup is the same as shown in Figure 4.3(b). The PC has an Intel® Core™ i5-3320M processor and RAMs of 4.00GB with Windows 10 Pro N 64-bit operating system. The images generated by the PC have a size of 250 x 250 pixels. The PC generates four images to represent each phase of the flame as shown in Figure 5.9. The white line object with a thick of 10 pixels was used as the object to represent a flame. For the image at expand phase, the line had a direction of 90° and a length of 100 pixels. At the appear phase, the system records the

ignition point and starts counting. At the expand phase, the system continues updating the elapsed time counter. At the steady phase, meaning that the length of the object does not change, the system stops updating but the the elapsed time counter is still counting. At the shrink phase, the system stops the counting and calculates the flame speed and the flame direction. At the disappear phase, the system resets the elapsed time counter and gets ready for the next object to occur.

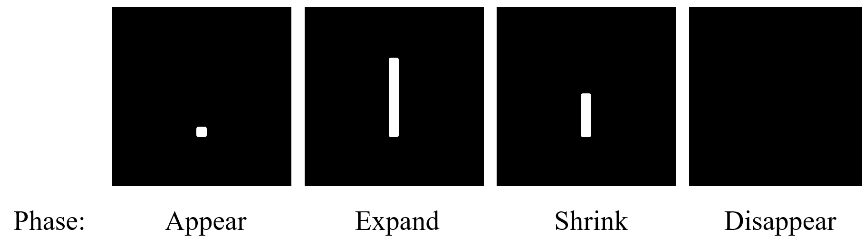


Figure 5.9: Image sequences for testing the implemented circuit

The duration between the appear phase and the expand phase was varied by the PC from 1 pixel/s to 5,000 pixels/s. The generated images were sent from the PC to the FPGA via serial communication with a speed of 921,600 bit per second (bps). Figure 5.10(a) shows the flame speed measurement of the motion object detection circuit in the FPGA. It shows that starting at the input speed of 166 pixel/s, the measured speed by the FPGA produced an error. This was caused by the PC's operating system that was not able to handle a real-time communication at the corresponding input speed. For testing the flame direction, the image sequence as shown in Figure 5.9 was applied

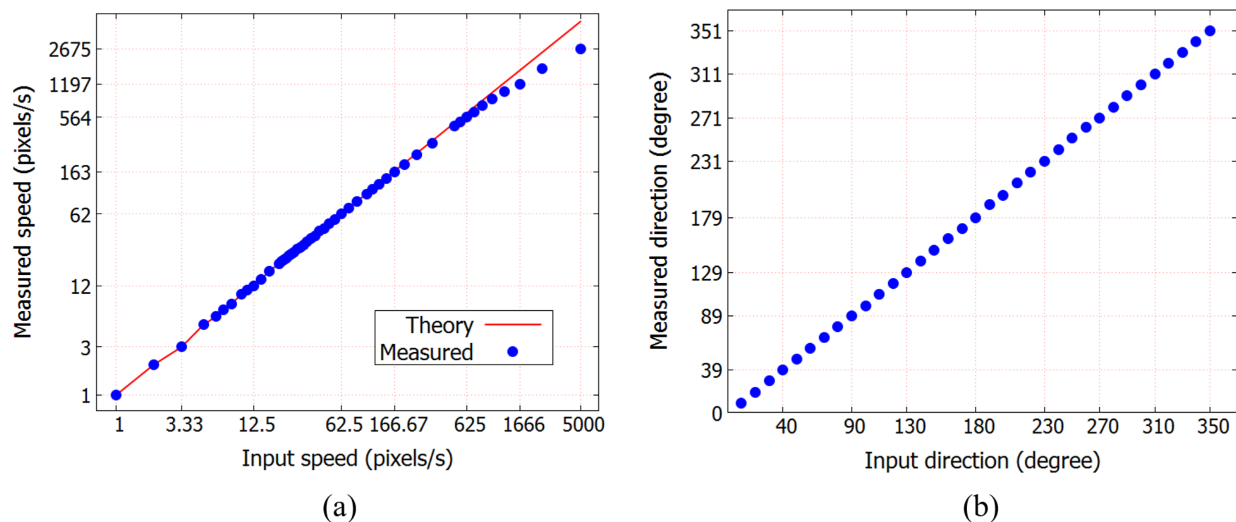


Figure 5.10: Simulation results for a two-dimensional array of 250 x 250 pixels. (a) Flame speed measurement. (b) Flame direction measurement

with the angle from the x-axis was varied from 0° to 350° with a step of 10°. Figure 5.10(b) shows the flame direction measurement. It shows that the system was able to measure the given flame direction.

5.3.2 One-dimensional array implementation result

For one-dimensional array implementation, the experimental setup is the same as shown in Figure 4.3(c). The fabricated 1 x 16 pixels EDC chip was integrated with the FPGA using wires. Each output pin of the EDC was connected to the input pins of the FPGA. The motion object detection circuit in the FPGA was modified to receive a one-dimensional array by forcing the horizontal projection values as 1s when there is an object in the image and 0s when there is no object. A microcontroller was used to simulate the focal plane array of 1 x 16 pixels. The microcontroller outputs logic-1s to represent a flame object and logic-0s to represent the image's background. The patterns generated by the microcontroller are as follows. The appear phase was "0100000000000000", the expand phase was "0111111111111110", the shrink phase was "0111110000000000", and the disappear phase was all zeros. The duration between the appear phase and the expand phase was varied and measured using an oscilloscope to define as the input

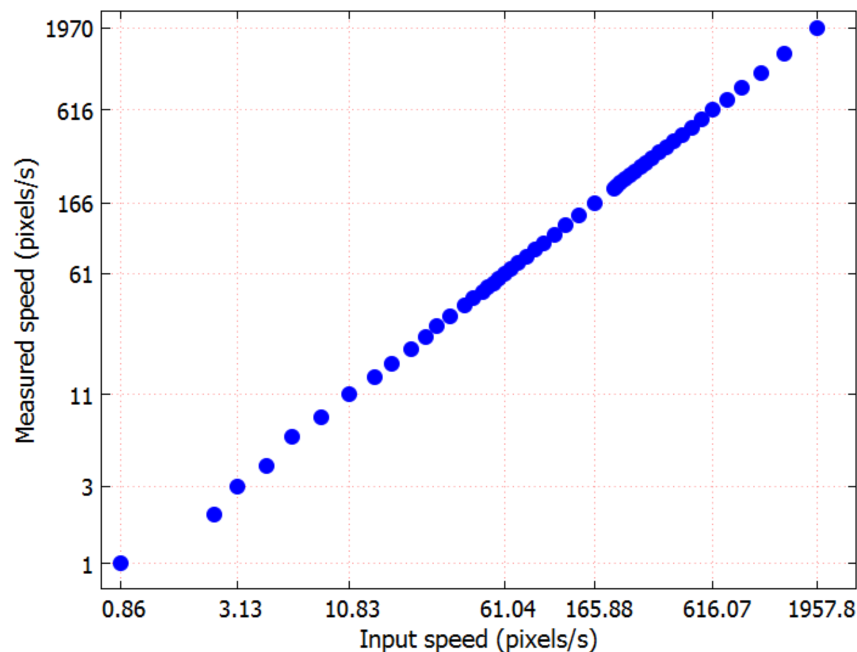


Figure 5.11: Speed measurement result of the integration between the fabricated 1x 16 pixels edge detection circuit chip and the FPGA.

speed. The measurement result of the motion object detection in the FPGA was sent to the PC to be recorded. Figure 5.11 shows the measurement result of the speed calculation. It is showed that the system was able to measure the given speed as low as 0.86 pixels/s up to 1,957.8 pixels/s. The use of the elapsed time counter makes the system having a wide range of the flame speed measurement comparing the previous method. The minimum and the maximum flame speed that can be measured are shown in eq. 5.8.

$$V_{min/max} = \frac{D_{min/max}}{T_{max/min}} \tag{5.8}$$

Here, $D_{min/max}$ is the displacement of the flame in pixel and $T_{max/min}$ is the elapsed time in second. For this one-dimensional array of 1 x 16 pixels system, the generated patterns had a displacement in a range of 1 - 13 pixels while the elapsed time counter register held a time in a range of 100 μs - 3 seconds. Thus, the minimum flame speed (V_{min}) that can be measured is (1 pixel / 3 s =) 0.33 pixel/s and the maximum flame speed (V_{max}) that can be measured is (13 / 100 μs =) 130,000 pixels/s.

The method for converting the pixel speed into the real speed is shown in Appendix C by assuming the system is using a simple lens in front of the sensor. If a biconvex lens with a focal length of 3 mm is added in front of the sensor then the pixel speed of 0.86 - 1,957.8 pixel/s would be equal to the real speed of 1.43 - 3,263 m/s. Adding a lens also affecting the reception of the photon flux. For instance, by using a lens with a focal length of 3 mm and a diameter of 1 cm, there will be a multiplication factor of 8.7 for the received radiation power.

5.3.3 Transmitted data length to support the IoT device

This smart UV sensor is designed to be fit as an Internet of Things (IoT) device concerning to the number of data being transmitted. To be an Internet of Things (IoT)-enabled device, the output of the smart UV sensor can be connected to a radio communication module on board. In order to have a small form factor, a battery-powered device is more desirable. The communication protocols for IoT devices have a low data rate as well as a small packet data to be transmitted/received to lower the power consumption.

Table 5.1 shows the comparison of the number of data to be transmitted when the system is implemented as a one-dimensional array of 1 x 16 pixels or as a two-dimensional array of 250 x 250 pixels. The ignition point estimates the original location of where the flame was formed.

Table 5.1: The number of data to be transmitted by the smart UV sensor

Transmitted information	**Array of 1 x 16 pixels**		**Array of 250 x 250 pixels**	
	Range	**Bit**	**Range**	**Bit**
Ignition point				
(x-axis, C_x)	1 - 16	5	1 - 250	8
(y-axis, C_y)	n/a	-	1 - 250	8
Projection coordinate				
(left side, R_V)	1 - 16	5	1 - 250	8
(right side, F_V)	1 - 16	5	1 - 250	8
(top side, R_H)	n/a	-	1 - 250	8
(bottom side, F_H)	n/a	-	1 - 250	8
Flame information				
Presence (alarm)	0 - 1	1	0 - 1	1
Speed	0 – 65,535	16	0 – 65,535	16
Direction	0 - 255	8	0 - 359	9
Spreading status	0 - 3 (twice)	4	0 - 3 (twice)	4
Communication related				
Checksum	0 - 255	8	0 - 255	8
Synchronization	0 - 255 (twice)	16	0 - 255 (twice)	16
Total bits		**68**		**102**

The projection coordinate informs the location of the flame as the rectangular shape within the observation (image) area. The presence information is used to generate an alarm when the flame occurs. The speed information calculates the flame speed just after the captured flame starts to shrink. The direction information tells where the flame was spread related from the ignition point. The spreading status notifies whether the flame is expanding, steady, shrinking, or lost from the observation area. The spreading status consists of two states which are the current status and the previous status. It is very useful for the system to know the previous status of the flame. For data framing purpose, checksum and synchronization were added. The checksum is used to verify the data integrity. The synchronization is used to tell the receiver when the data entities start and end.

From the Table 5.1, the 1-D array of 1 x 16 pixels requires 68 bits or 9 bytes of data while the 2-D array of 250 x 250 pixels needs 102 bits or 13 bytes of data to be transmitted from the smart UV sensor. This number of data is suitable as the payload of the Bluetooth low energy (BLE) for instance. The BLE has a payload of ∼20 bytes or ∼160 bits. [69] This confirms that the number of data generated by the smart UV sensor is applicable to an IoT device. Further scaling by increasing the number of pixel of the sensor mainly grows the number of bit of the ignition point as well as the projection coordinate.

5.4 Conclusion

The wired-integration system between the fabricated EDC chip of 1 x 16 pixels and the FPGA has been described. The PC and the microcontroller was utilized for substituting the focal plane array to generate the binary images or the patterns. In the first model as described in Chapter 4, the system was evaluated to calculate the speed of the moving object and its direction. It is shown that the system was able to measure the speed of the moving object at 1.7 - 2,049 pixels/s with different sampling frequency in a range of 1 - 200 Hz. In the second model, the system was evaluated to calculate the speed of the spurt object. The calculation method is modified by adding an elapsed time counter. As a result, the system was able to measure the speed in a range of 0.86 - 1,957.8 pixels/s which is equal to the speed of 1.43 - 3,263 m/s. The one-dimensional array of 1 x 16 pixels generated 68 bits of information to be transmitted from the smart UV sensor. This confirms that the designed smart UV sensor is sufficiently fit as the IoT device.

Chapter 6

Concluding remarks and recommendations for future work

6.1 Concluding remarks

This research has developed a smart UV sensor for hydrogen flame application based on neuro-OEIC and FPGA. The smart UV sensor extends the application of the fabricated UV focal plane array. The monitoring system in an area where hydrogen is being used requires a real-time processing and low-power consumption. The neuro-OEIC extracts the edge of the captured flame object for reducing the pixels being activated. Hence, it leads to a power reduction. The structure of the neuro-OEIC that is stacked onto the FPGA enabling the 3-D integration architecture to realize a real-time data transfer. The FPGA itself is used as an image analyzer for substituting the computer system. Therefore, a small size of sensor with low-power consumption can be achieved.

A few notable finding in this research are as follows:

1. The neuro-OEIC extracts the edge of the captured flame instantly. No clock is required since it is an analog circuit. Having a preprocessing unit as edge extractor is very useful in the flame analysis field, especially to recognize the shape of the flame. Even though the flame's shape recognition is not implemented in this research, the edge detection circuit reduces the number of pixel being activated. Therefore, it also has a ability for reducing the power consumption.

2. The use of histogram projection for simplifying the shape of the flame into a rectangular shape is valuable. Although it does not inform the exact area of the flame, but it gives a fast processing time to obtain the vector resultant of the flame, comparing to the optical flow methods. A fast processing time means that the system might have a real-time performance for processing a high-speed flame object.

3. In the spurt model, the system could measure a wide range of flame speed without changing the sampling frequency. This is suitable for real application since no parameter is adjusted

for any kind of flame speed value in a range of the detectable speed. The concept of sampling frequency was changed to the use of the elapsed time between the appear phase and the expand phase. The base clock period and the size of the register that holds the counting determine the range of the measured flame speed.

4. A basic lens equation gives useful information about estimating the sensor resolution, converting the pixel speed to the real speed, as well as increasing the received radiation power.

5. The 3-D integration architecture concept offers a great opportunity for delivering the data from the sensor to the FPGA in parallel. A parallel data transfer leads to a real-time performance. Despite the current SSI technology does not stack a die/chip onto the FPGA logic, hopefully in the near future a custom of true 3-D stacking can be realized.

6.2 Recommendation for future work

Throughout the lengthy research process, we have identified several pointers that we can recommend as possible direction for future researches in this particular topic, as follows:

1. Stacking the photodiode and the edge detector circuit requires a matching area. Currently, the fabricated EDC chip has an area size of 875 μm x 600 μm with 5 micron design rules, while the previous fabricated SBD UV photodiode had been optimized for an area size of 250 μm x 250 μm. By decreasing the design rules from 5 to 1 micron, the EDC can have an area of

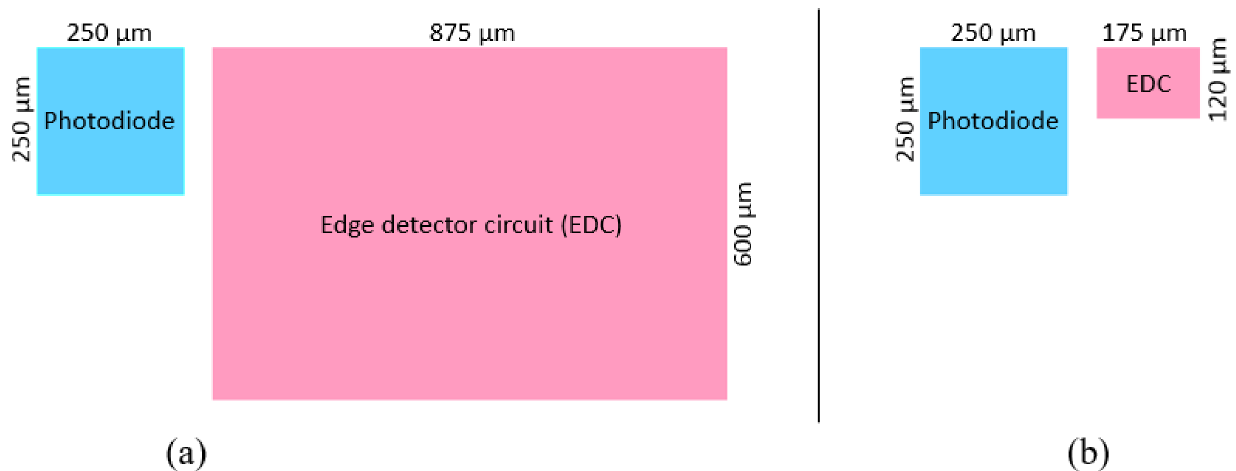


Figure 6.1: Scaling the edge detector circuit to match with the existing photodiode. (a) Using 5 micron design rules. (b) Using 1 micron design rules

175 μm x 120 μm, which is sufficient fit under the existing photodiode for one pixel. Figure 6.1 shows the comparison of area scaling between the EDC and the fabricated photodiode.

2. In this stage, the working range of the fabricated EDC is above the requirements. Further work might investigate some methods that can be applied. The methods are scaling down the EDC for increasing the open circuit voltage at the silicon diode, adding amplifier to amplify the photocurrent, or multiplying the incident photon by adding a bigger lens.

3. In the design of the neuro-OEIC, it produces undetected edge when the object occurs in the boundary of the sensor area. This is caused by the absence of the horizontal network since there is no neighbor pixels at one of its side. In one-dimensional array, this issue produces a false information regarding to the size of the object. Further work could be modification of the horizontal network. Whether by adding horizontal networks that are connected to a specific potential or adding a dummy pixel with zero photocurrent might solve this issue.

4. There is a case when the size of the object is larger than the image area. This could be happened when the hydrogen flame occurs at a short distance from the sensor or the actual size of the hydrogen flame is indeed large, the EDC will not generate edges. Then, since there is no edge signal from the EDC, the motion object detection circuit in the FPGA decides this condition as no object. As a result, the system fails to detect the presence of the hydrogen flame. Further work could be adding an additional circuit for sensing whether the level of the photocurrent is above the threshold to trigger a dedicated signal to the FPGA circuit indicating that the UV-C radiation is present.

5. In the motion object detection circuit, it only detects a single object within the image. Using histogram projection algorithm creates fragmented image. Further work could be implementing a clustering algorithm for counting the number of object.

6. In the spurt model, the system algorithm restarts the measurement of the flame speed after the object disappear from the image. In case of second explosion or more, the system can not measure the flame speed. Further work could be adding an algorithm to handle this issue.

7. In the future, the application of this smart UV sensor might be extended not only detects the hydrogen flame, but also detects another invisible flames such as sulfur flame or metal-based flame, as long as they generate UV-C radiations.

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Appendices

A. Silicon as UV detector

The bandgap energy of a silicon or other materials depends on the temperature and experimentally determined as shown in eg. A.1 [70],

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{A.1}$$

Here, $E_g(0)$ is the bandgap energy at absolute zero Kelvin, α and β are material specific constants. For silicon, the value of $E_g(0)$, α, and β is 1.170 eV, 0.473 meV/K, and 636 K, respectively. So, at temperature of 273 K, a silicon has a bandgap energy of 1.13 eV. Therefore, a silicon is associated as a narrow bandgap material. Then, by using the Planck-Einstein relation as shown in eq. A.2, the cut-off wavelength, which is the maximum detectable wavelength, of a given bandgap can be calculated.

$$E_g = h\nu = \frac{hc}{\lambda} \tag{A.2}$$

Here, E_g is bandgap energy, h is Planck's constant ($6.63x10^{-34} Js$), ν is the frequency in Hertz, c is the speed of light ($3.0x10^8 m/s$), and λ is the cut-of wavelength.

B. Photodiode design calculation

The expected detection range of the photodiode was 10 pW/mm^2 – 10 μW/mm^2. The lowest radiation power of 10 pW/mm^2 is a lighter at 10 m away from the photodiode (without an optical subsystem). The photocurrent generated by the photodiode can be expressed as in eq. B.1,

$$I_{PH} = SN\eta q \tag{B.1}$$

Here, S is the incident light area in meter square, N is the number of incident photon per second per square area, η is the external quantum efficiency, and q is the elementary particle charge ($= 1.602 \times 10^{-19}$ C). By assuming the hydrogen flame is a dot source which its light energy travels to all directions uniformly like a sphere, and the photodiode crosses the inner surface of the sphere, then the number of incident photon is calculated by dividing the radiation power per unit time falling on the area of the photodiode with the average energy per photon as shown in eq. B.2,

$$N = \frac{P}{E_g} = P\frac{\lambda}{hc} \tag{B.2}$$

Here, P is the radiation power at the photodiode in Watt per square area, λ is the photon wavelength, h is the Planck' constant ($= 6.626 \times 10^{-34}$ Js), and c is the speed of light ($= 3.0 \times 10^{8}$ m/s). By substituting eq. 3.4 into eq. 3.3, we got eq. B.3.

$$I_{PH} = SP\frac{\lambda}{hc}\eta q \tag{B.3}$$

Let the area of the designed photodiode S is equal to 250 $\mu m \times 250$ μm ($= 6.25 \times 10^{-8}$ m^2), the wavelength of the UV source λ is 280 nm ($= 2.8 \times 10^{-7}$ m), h times c is equal to $1.9864748 \times 10^{-25}$ J.m, and q is $= 1.602 \times 10^{-19}$ C, the generated photocurrent can be calculated as in eq. B.4.

$$I_{PH} = 14.113 \times 10^{-9}\frac{m^2.C}{J} \times \eta \times P \tag{B.4}$$

To calculate the efficiency of the fabricated photodiode, the radiation power density on the photodiode's surface is calculated using eq. B.5.

$$P = \frac{I_{PH}}{\Re} \times \frac{1}{S} \quad \text{(B.5)}$$

Here, P is the radiation power at the photodiode in Watt per square area, I_{PH} is the photocurrent generated by the photodiode in Ampere, $\Re$ is the responsivity in Ampere per Watt, and S is the area of the photodiode in square meter. The previous fabricated BSI-SBD photodiode of $250\ \mu m \times 250\ \mu m$ under illumination with the wavelength of 296 nm showed a photocurrent of 8×10^{-11} A and a responsivity of 2×10^{-4} A/W. Thus, the radiation power (P) is 6.4 μW/mm^2.

By substituting a radiation power of 6.4 μW/mm^2 and a photocurrent of 8×10^{-11} A to eq. 3.6, this results the efficiency of the fabricated photodiode is 0.0008857 or $\sim 0.1\%$. In this current stage, the photodiode achieves a relatively low efficiency. However, the efficiency of the AlGaN-based photodiode will become better in the near future.

Table B.1 shows the generated photocurrent for the minimum and maximum radiation power between the fabricated photodiode that provided an external quantum efficiency of 0.0008857 and the expected photodiode with an external quantum efficiency of 0.1. The minimum radiation power is 10 pW/mm^2 ($= 10 \times 10^{-12}$ W/10^{-6}m^2 $= 1 \times 10^{-5}$ W/m^2 $= 1 \times 10^{-5}$ J/s.m^2) and the maximum radiation power is 10 μW/mm^2 ($= 10 \times 10^{-6}$ W/10^{-6} m^2 $= 10$ W/m^2 $= 10$ J/s.m^2). The fabrication photodiode had a dark current of 10^{-13} A, which is equal to the radiation power of 8 nW/mm^2. Therefore, the detection limit of the fabricated photodiode, that was defined as 10 times of the leakage current, is 80 nW/mm^2.

Table B.1: Generated photocurrent without optical subsystem

Radiation power	**Fabricated photocurrent η=0.1%**	**Expected photocurrent with η=10%**
10 pW/mm^2 (minimum)	0.125 fA	14.113 fA
8 nW/mm^2	0.1 pA (dark)	-
10 μW/mm^2 (maximum)	0.125 nA	14.113 nA

C. Lens and illuminance of an image

Lens is a piece of glass or other transparent material with curved sides for focusing or spreading light rays, used singly (as in a magnifying glass) or with other lenses (as in a telescope). For this smart UV sensor, a biconvex lens might be used to increase the number of photon flux that hits the photodiode. There are two topics about the lens that are used in this doctoral thesis. The first is about the field of view relationship to calculate the minimal number of pixels or sensor resolution. The second is to calculate the amount of illuminance on the sensor.

C.1 Sensor resolution estimation

The relationship between field of view and the focal length of the lens can be used to estimate the sensor resolution or the number of pixel for one-dimensional array. Figure C.1 shows the placement of the lens between the object and the sensor. Eq. C.1 shown the relationship between the object and the projected object in the sensor.

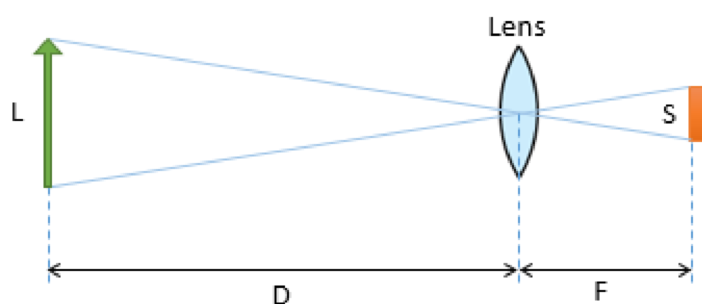


Figure C.1: Field of view of a lens

$$\frac{S}{L} = \frac{F}{D} \tag{C.1}$$

Here, S is the sensor length, L is the length of the object or the vertical field of view, F if the lens focal length, and D is the distance of the object from the lens.

Let the length of the object (in this case is the hydrogen flame) is 5 m, the lens focal length is 3 mm, and the distance is 10 m. Then, the sensor length is ($\frac{5m}{10m} \times 3mm =$) 1.5 mm.

The illustration to count the number of pixel is shown in Figure C.2. The number of pixel (N) is equal to the sensor length (S) divided by the pitch (S)of the sensor as in Eq. C.2.

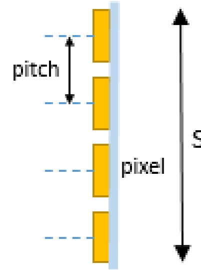


Figure C.2: Pixel pitch at the sensor's surface

$$N = \frac{S}{P} \tag{C.2}$$

For a sensor length of 1.5 mm with a pith of 500 μm, the number of pixel is 3 pixels. This result shows that the minimum pixel for a sensor with one-dimensional array is 3 pixels. Thus, for a sensor with two-dimensional array, the minimum pixel resolution would be 3 x 3 pixels. To have a better coverage of the flame, it is adequate to construct the number of pixel at two times of the N-number. However, the pixel's pitch defines the smallest object that can be detected. In the above example, a pitch of 500 μm means that the smallest detectable object's length from 10 m away is 1.7 m.

The relationship between the actual flame speed and the pixel speed also can be derived, as shown in Eq. C.4. For instance, a flame with a speed of 100 m/s reaching a height of 5 m will take 50 ms. Therefore, on the sensor's surface, the pixel speed will be 3 pixels/50 ms or 60 pixel/s.

$$V_P = N \times \frac{V_F}{L} \tag{C.3}$$

Here, V_P is the pixel speed in pixel/s, N is the number of pixel, V_F is the actual flame speed in m/s, and L is the defined length of the flame in m.

C.2 Photon flux multiplier

A lens might be used for focusing the object on the sensor's surface. The lens is also applied to multiply the photon flux on the sensor's surface. Figure C.3 shows the formation of an image by a simple lens. The relationship between the luminance and the illuminance is shown in Eq. Luminance or brightness is the luminous intensity per unit area of light traveling in a given direction. Luminance describes the amount of light that passes through, is emitted or reflected from a particular area, and falls within a given solid angle. Illuminance is the total luminous flux incident on a surface per unit area. In this discussion, luminance is related to the flame source and illuminance is related to the sensor.

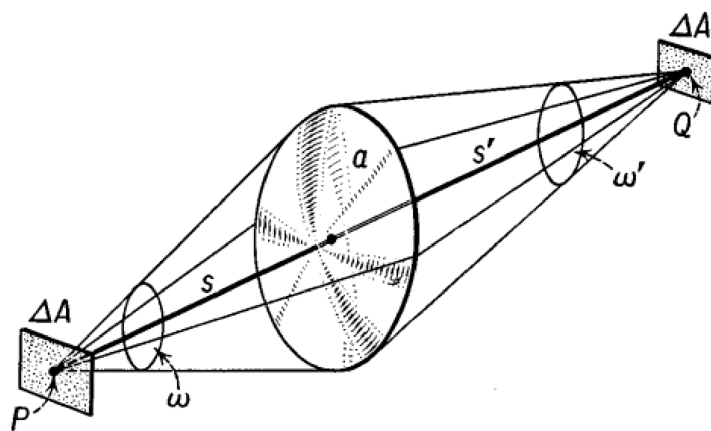


Figure C.3: Formation of an image by a simple lens. *Source*: H. Semat and R. Katz, "Physics, Chapter 38: Mirrors and Lenses" (1958), Robert Katz Publications, p. 719

$$E = B \times \frac{\pi}{4} \times \left(\frac{a}{s'}\right)^2 \tag{C.4}$$

Here, E is the illuminance, B is the brightness, a is the diameter of the lens, and s' is the lens focal length. A lens with a focal length of 3 mm and a diameter of 1 cm will result $E = 8.7 \times B$. While a lens with the same focal length and a diameter of 3 cm will result $E = 78.5 \times B$. This concludes that using a lens with a focal length of 3 mm and a diameter of 3 cm will increase the photocurrent of the fabricated photodiode with a factor of 78.5.

D. Vacuum pumps

Achieving a ultrahigh vacuum condition, a vacuum system needs at least two pumps: a roughing pump and a high-vacuum pump. A roughing pump works in the viscous flow regime and a high-vacuum pump works in the molecular flow regime. Viscous and molecular flow regimes are gas flow regimes that were defined as a function of system dimension and pressure. The connection between those two pumps is called as foreline and their operation is called fore-vacuum. Figure D.1 shows the vacuum chamber in a typical vacuum system. A typical vacuum system for a high vacuum or ultrahigh vacuum usage is shown at Figure D.2.

Roughing pumps and high vacuum pumps are distinguished by the pressure that can be achieved. They are also grouped by their operation principle into gas transfer pumps and entrapment pumps. Figure D.3 shows the classification of vacuum pumps. Gas transfer pumps eliminate gas molecules from the vacuum chamber by taking them out in one or more steps of compression. Gas transfer pumps can be formed as displacement pumps or kinetic transfer pumps. Rotary vane pump, piston pump, lobe/roots pump, and diaphragm/membrane pump are the example of displacement pump and they are used as roughing pumps in a vacuum system. Diffusion pump, turbomolecular pump, and turbomolecular drag pump are the example of kinetic transfer pumps and they are used as high and ultrahigh vacuum pumps. Instead of removing gas molecules forever, entrapment pumps

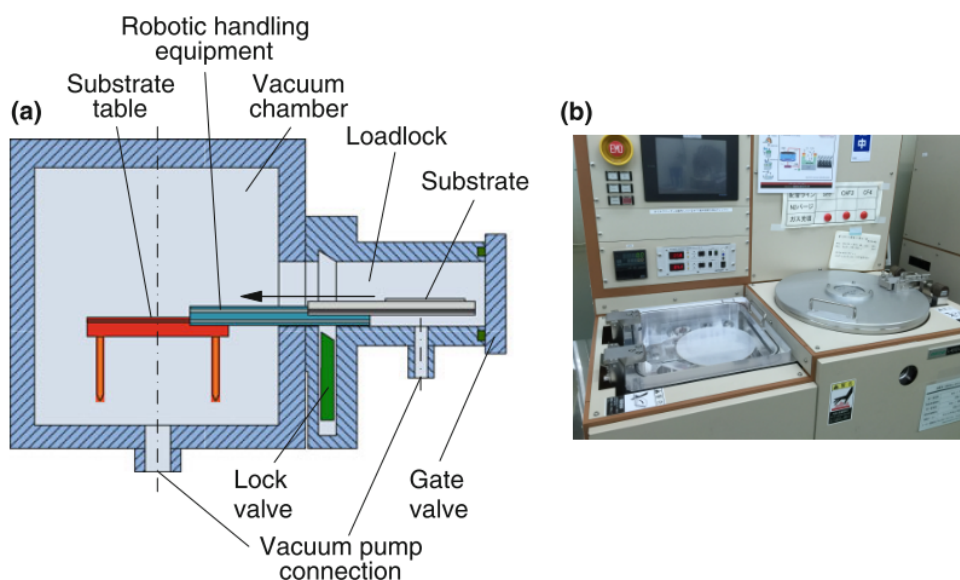


Figure D.1: A vacuum chamber with a loadlock. (a) Diagram of a loadlock (frontloaded). [57] (b) Loadlock (toploaded at the left side) of a etching machine (RIE). *Photograph*: Clean Room, Toyohashi University of Technology

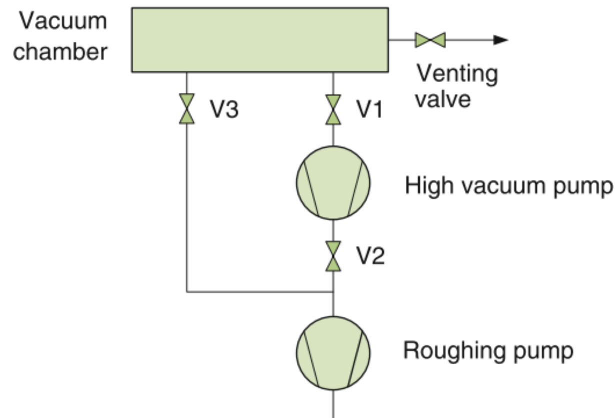


Figure D.2: A typical diagram of a high vacuum or ultrahigh vacuum usage. V1, V2, and V3 are valves [57]

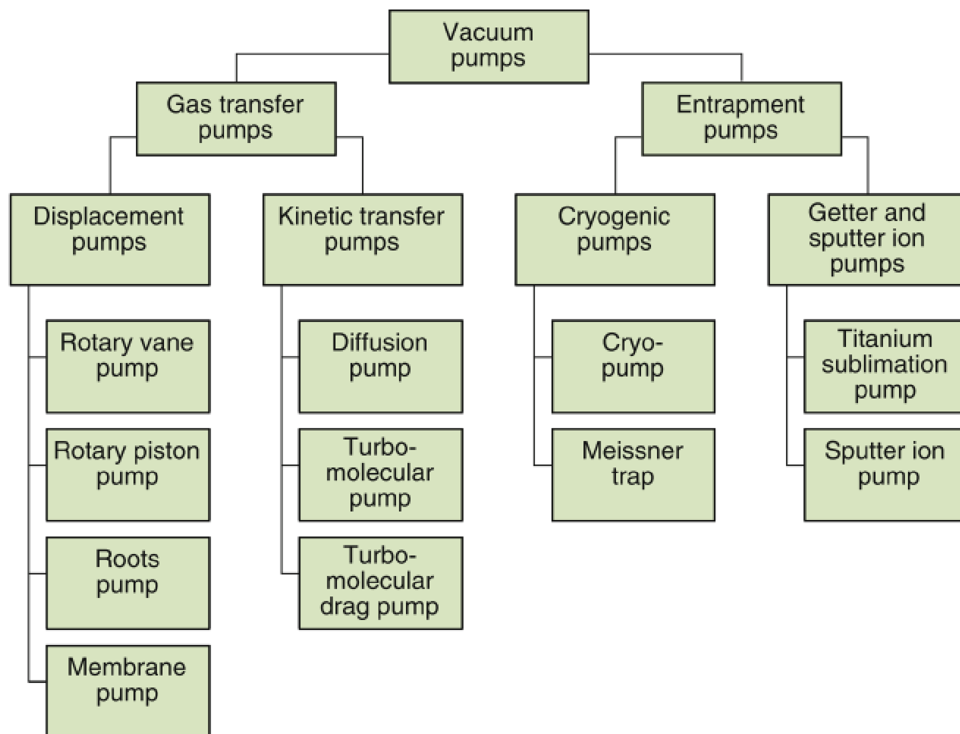


Figure D.3: Classification of vacuum pump [57]

works by trapping the gas molecules in a solid or absorbed condition within the vacuum chamber. Some of them (cryopump and Meissner pump) works reversible to release the trapped gas back into the system. Entrapment pumps are auxiliary pumps to increase the high vacuum performance. High vacuum pumps start after roughing pumps has lowered the pressure in the vacuum chamber to fore-vacuum in the rough or medium vacuum range. Figure D.4 shows the industrial vacuum

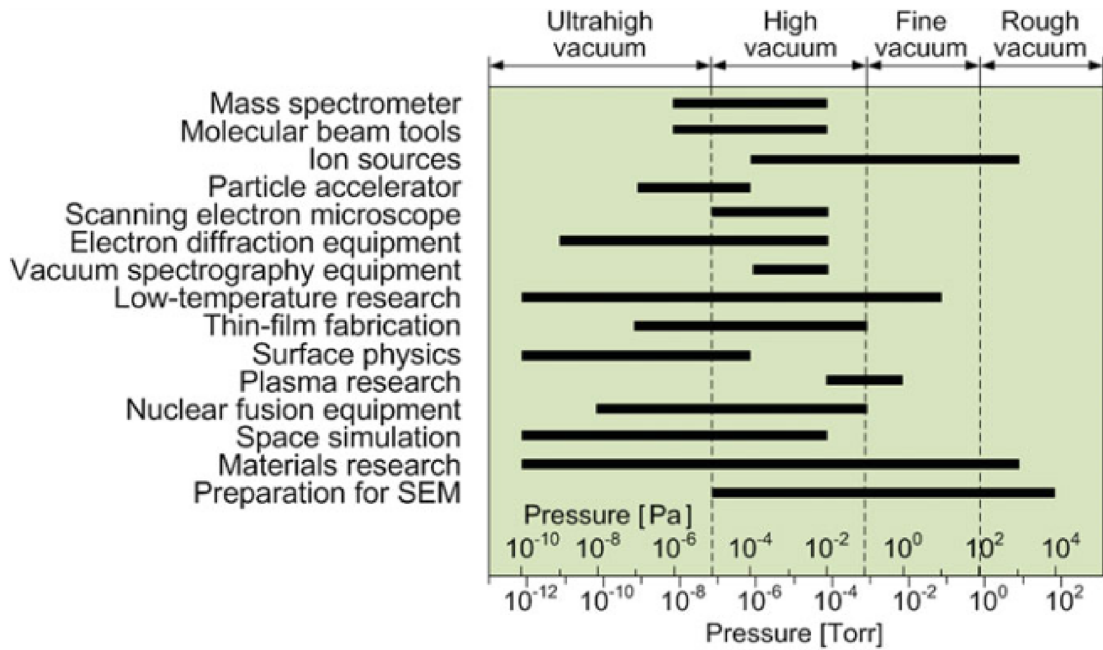


Figure D.4: Industrial vacuum application [57]

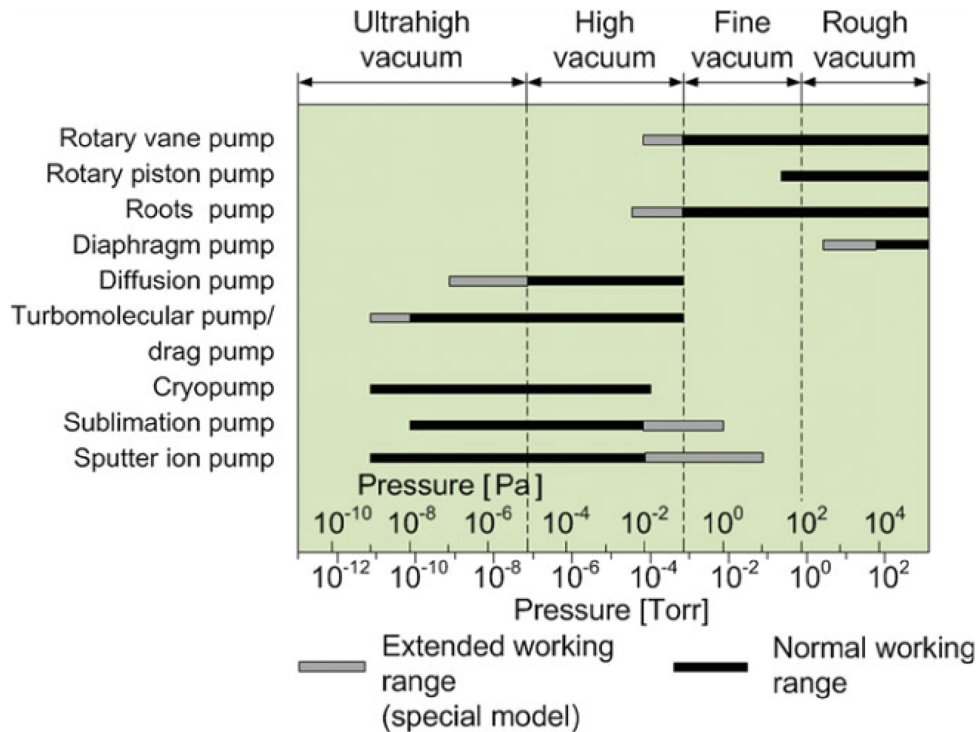


Figure D.5: Operation range of vacuum pump [57]

application and Figure D.5 shows the operation range of vacuum pump.

Roughing pump can be oil-sealed pumps or dry pumps. In oil-sealed roughing pump, oil is used for sealing and lubricating the vacuum. Thus, it may cause hydrocarbon back streaming which may disturb some fabrication process. A rotary vane pump and a rotary piston pump is an oil-sealed pumps. There is a special corrosion resistance vacuum oil when corrosive gases are used, such as Fomblin®, a perfluoro-polyester (PFPE). A lobe blower, better knows as a root pump, is used in connected before a rotary vane or piston pump since it can not work against the atmospheric pressure. A diaphragm pump is oil-free pump but it has a low fore-vacuum pressure which will require a special high vacuum pumps.

In high vacuum pumps group, there is a diffusion pump which is actually a vapor jet pump. It used a high-speed vapor stream that collides with the gas molecules. The main advantages is there is no moving parts. Commonly, hydrocarbon oil is used as pumping fluid. Therefore, it may contaminate the fabrication process. Also, it is prohibited to pump corrosive gases and pure oxygen which will result an explosion. Thus, integrating with a Meissner pump can be an alternative. A turbomolecular pump has special blades at both rotor and stator which each pair represents one stage of the turbomolecular pump. The blade speeds are in the same range with the velocity of gas molecules. Hence, the gas molecules are sucked from the inlet to the outlet. Because of the high speed rotation, high-performance bearing is needed in three options: oil-lubricated ball bearings with steel balls only for vertical installation, grease-lubricated hybrid bearings, and magnetic levitation bearings. The last one wear-free, maintenance-free, direction-free, and hydrocarbon-free. When corrosive gases are used such as chlorine or fluorine, usually the bearings are flooded with inert gas (for example, N_2). A turbomolecular drag pump was designed by adding a molecular drag pump stage on the axis of the turbomolecular pump at its high pressure end. The reason is when a diaphragm pump and a magnetically levitated turbomolecular pump is combined to create a oil-free system, the diaphragm pump can not reach the fore-vacuum for the turbomolecular pump.

A cryopump uses compressed helium gases to create a cold area down to 4.2 K (it might have up to three stage of cooling: 80 K, 15 K, and 4.2 K) so that the gas molecules in the vacuum chamber can be condensed and absorbed. Since this pump works by capturing, it does not have gas outlet, and it may saturated. During the pump in off state, the pump is in regeneration condition where the trapped gases are released, in this case, cryopump does not support pumping corrosive gases. The cryopump has remote compressor with flexible hoses to minimize the vibration from the compressor.

A Meissner trap pump work as an inexpensive and simple cryo method. It uses liquid nitrogen

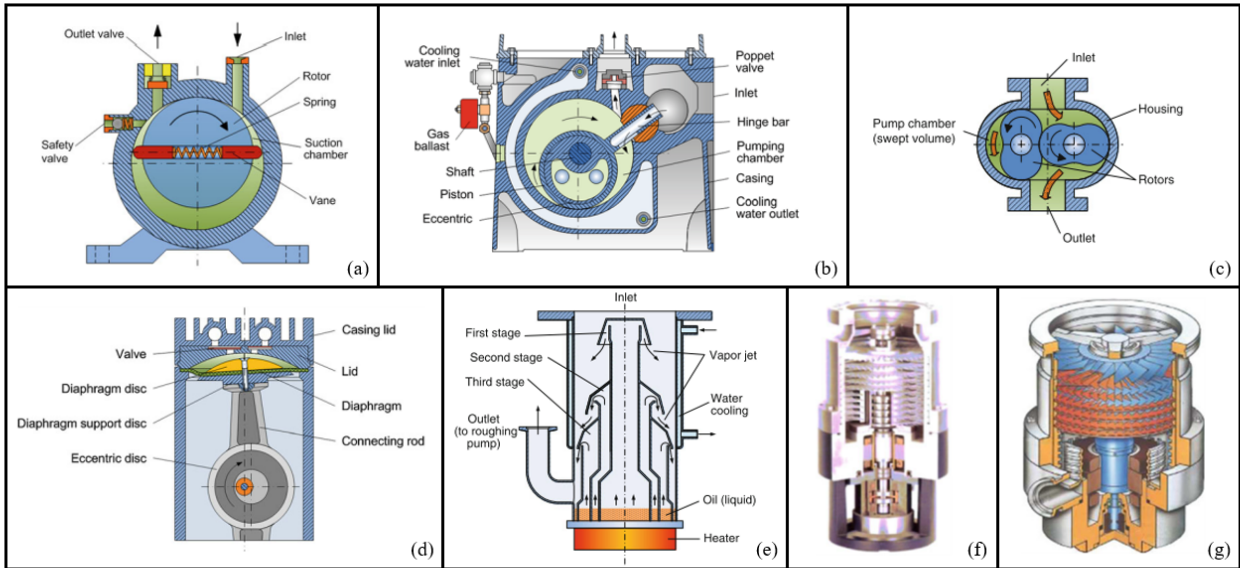


Figure D.6: Gas transfer pumps. (a) Rotary vane pump. (b) Rotary piston pump. (c) Root pump. (d) Diaphragm pump. (e) Diffusion pump. (f) Turbomolecular pump. (g) Turbomolecular drag pump [57]

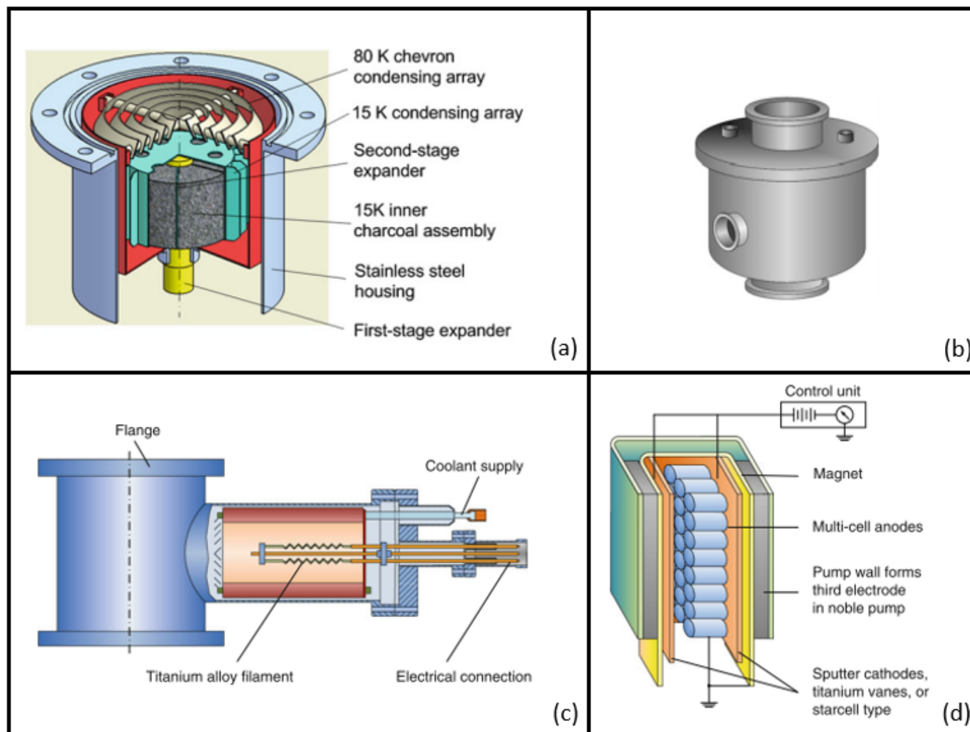


Figure D.7: Entrapment pumps. (a) Cryopump. (b) Meissner trap. (c) Titanium sublimation pump. (d) Sputter ion pump [57]

(LN_2) to cool down the gases at 77 K. Another entrapment pumps are getter pumps and sputter ion pumps. A getter pump is a titanium sublimation pump. The titanium vapor creates a Ti layer to trap reactive gases, thus this pump removes the gases permanently. A sputter ion pump uses a cold cathode electrical discharge to sputter the titanium plates which at the end reacted with reactive gases, such as N_2, O_2, and H_2.

One of the important parts in the vacuum equipment is vacuum seals, to avoid gas leakage into the vacuum chamber from the outside while vacuuming is on progress. Common used vacuum seal is O-rings made from elastomer which is a natural or synthetic polymer having elastic properties, e.g., rubber. Improving the sealing ability, lubricating by high vacuum grease is necessary to fill up the holes or space if exist. Metal seals are used when the high thermal is applied. Copper, aluminum, indium, silver or gold are used as metal seals. During operation, it is necessary to know the current pressure inside the vacuum chamber. Reading instruments used to monitor the pressure inside the vacuum chamber are Bourdon gauge, diaphragm gauge, and capacitance manometer for direct reading, pirani gauge, thermocouple gauge, Penning gauge, and Bayard-Alpert gauge for indirect reading. Finally, by considering the ability of each pump, a proper vacuum system can be performed.

E. Cleanroom design

A cleanroom is an environment with controlled contaminant. Since the size of the fabricated devices are small (in this thesis work, 1.5 μm process technology and 5 micron design rule was used), it is necessary to remove the contaminant before processing and avoids contamination by performing the fabrication in a cleanroom. Figure E.1 (a) illustrates the contaminants size comparing to a 1 μm micro structure and Figure E.1 (b) shows the cleanroom classification by U.S. Federal Standard (FS) 209D. The cleanroom classification was determined by the allowable particle size per cubic foot that exist in the ambient air. The number of particle was measured with no one presents in the cleanroom.

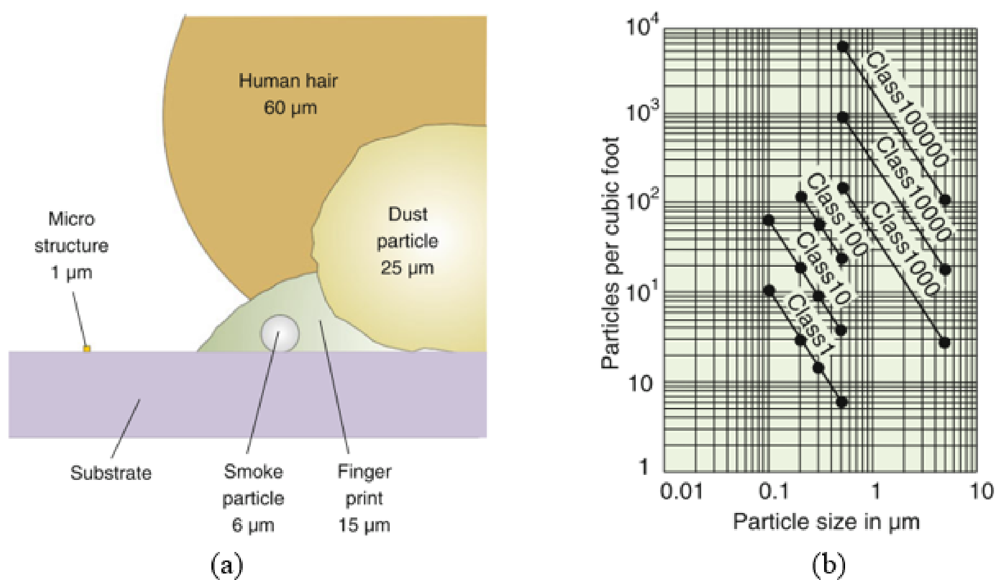


Figure E.1: Particle contaminant size. (a) Size comparison. (b) Cleanroom classification [57]

An air filtration system is important for the cleanliness of the cleanroom. High Efficiency Particulate Air (HEPA) filters and for strict requirements Ultra Low Penetration Air (ULPA) filters are used. Class 10 or lower uses ULPA filters, while Class 100 uses HEPA filters. A typical cleanroom's air distribution system is shown in Figure E.2. Air conditioning is used because the cleanroom needs a constant temperature at typically 22 °C and humidity at typically 40 % ± 5 %. A laminar air flow (where air travels in parallel streamlines) is currently used. A laminar air flow prevents particle from outside entering the flow area.

A cleanroom layout might have a ballroom type. A ballroom type has a big area without separator, hence lithography and other fabrication equipment are under yellow light and easily

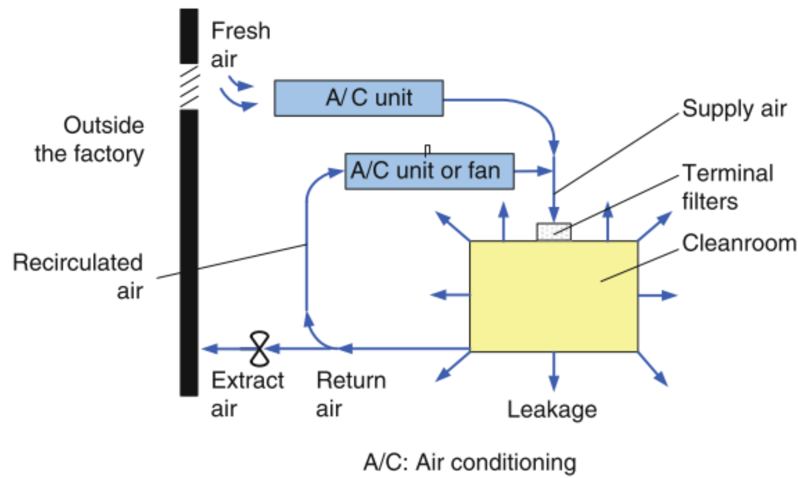
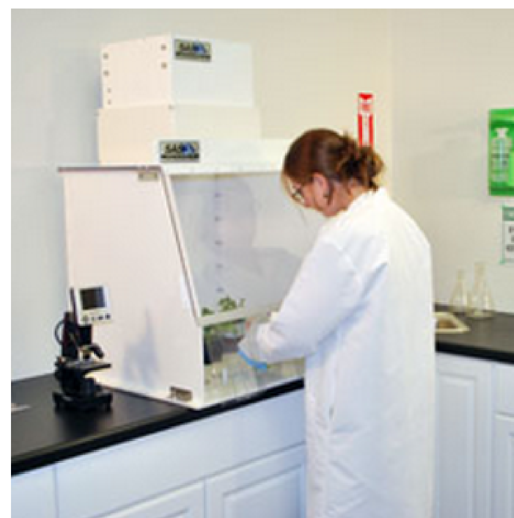


Figure E.2: A typical cleanroom's air distribution system [57]

moves the production tools between fabrication process. However, it consumes a lot of clean air supply. A low cost cleanroom might utilize a modular or mini environment type of cleanroom. It provides a clean air on a specific area. For moving the production tools between processes, a clean container can be used. Figure E.3 shows a modular cleanroom and portable cleanroom examples.

Another things as considerations when preparing a cleanroom are including the de-ionized water supply for many cleaning processes, dried nitrogen gas for blowing or cleaning, layouting between process units to make efficient movements or reduce the equipments vibration from the

(a)



(b)

Figure E.3: Small size cleanroom. (a) Softwall modular cleanroom. (b) Portable cleanroom. Both are manufactured by Terra Universal *(http://www.terrauniversal.com)*

blowers or pumps, emergency shower and eyewash in case of chemical accident, standard operation procedure or manuals operation of the equipments, waste disposal circulation, cleanroom garment including safety wearing when dealing with acid or alkali solutions, and air shower at the entrance of the cleanroom if needed.